

Model Name: GA-Z97MX-Gaming 5

Rev 1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A 1,2
08	DDR III CHANNEL B 1,2
09	PCH_FDI,DMI,USB,PCIE
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS X8 SWITCH
17	PCI EXPRESS X1/X4 SLOTS
18	IT8620 LPC IO
19	-PROHOT,RUSB,KB/MS
20	DUAL BIOS
21	IR 3564-PWM
22	IR VCORE
23	CODEC ALC1150
24	REAR AUDIO JACK
25	DISCRETE POWER&USB OV PROTECT&NCT3933
26	FP , FUSB
27	ATX

SHEET

TITLE

28	HWM,FAN CTRL
29	PCH HDMI/DVI
30	Bigfoot E2201 LAN
31	DDR15V
32	M.2 & SATA_EXPRESS
33	Amplifier Power

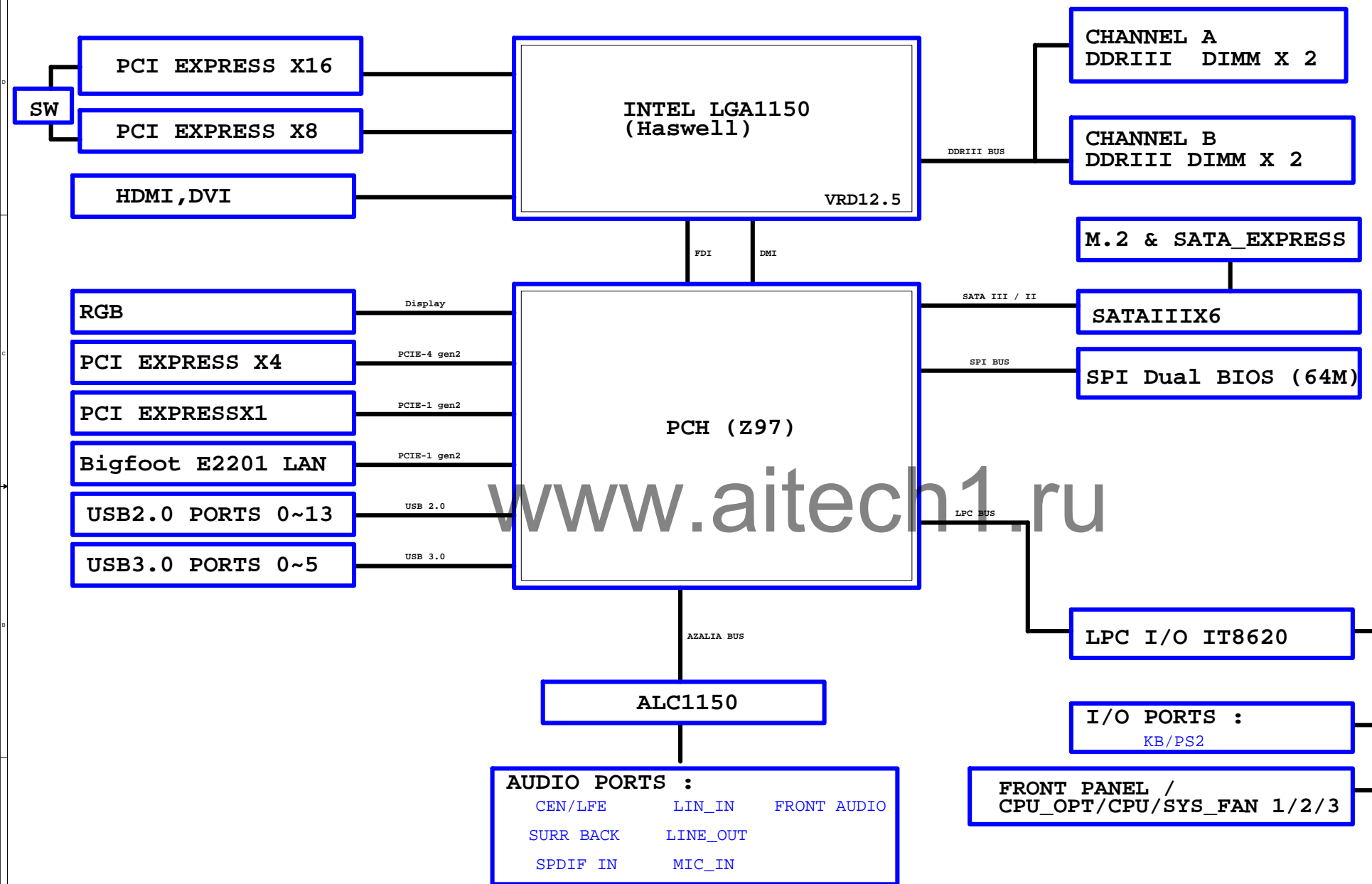
www.aitech1.ru

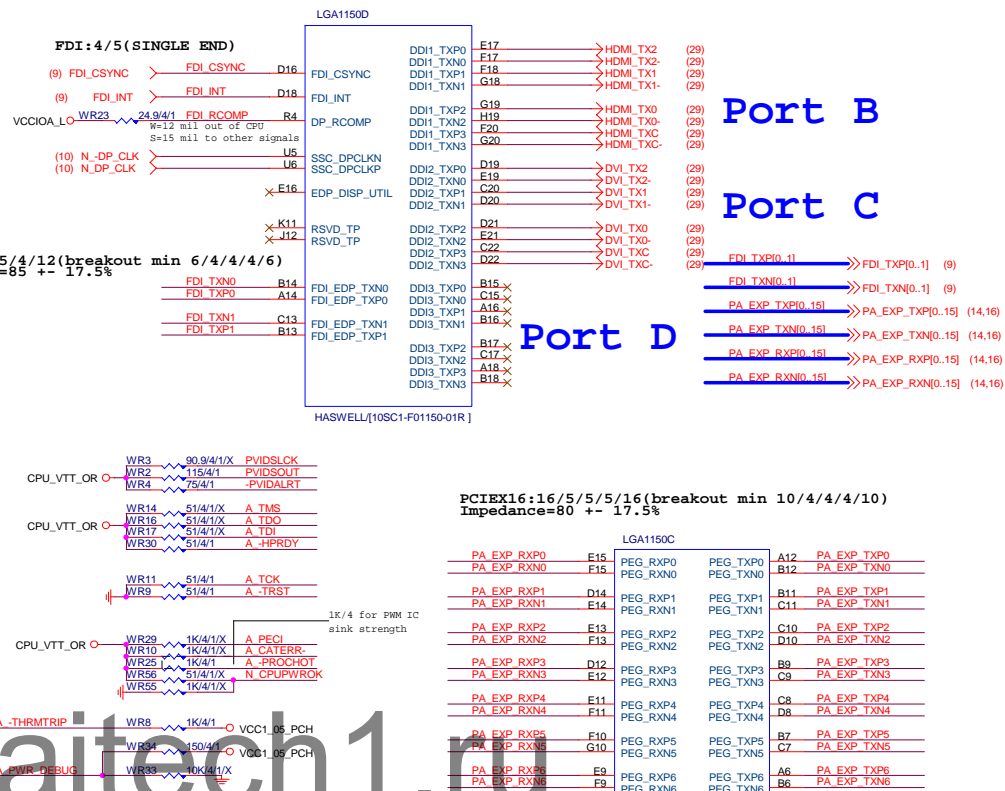
PCB:咖啡黑

Layout:angela 1960
RDPM: Nancy 1911/2345

Gigabyte Technology		
Title		
Cover Sheet		
Size	Document Number	Rev
Custom	GA-Z97MX-Gaming 5	1.0
Date:	Monday, May 12, 2014	Sheet 1 of 34

BLOCK DIAGRAM





$A_{-}CPURST \rightarrow A_{-}CPURST \quad (11)$



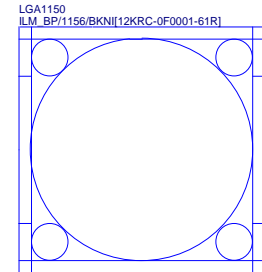
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Size	Document Number		Rev
Custom		GA-Z97MX-Gaming 5	1.0
Date:	Monday, May 12, 2014	Sheet	4 of 34

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MODT_A2	AW9	DDR0_ODT2	DDR0_DQ19	AF39	MDA19				
MODT_A3	AU8	DDR0_ODT3	DDR0_DQ20	AM37	MDA20				
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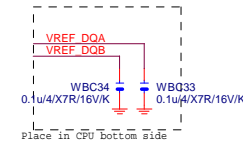
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MAAB7	AV26	DDR1_MA7	DDR1_DQ7	AH34	MDB7				
MAAB8	AU26	DDR1_MA8	DDR1_DQ8	AL34	MDB8				
MAAB9	AW25	DDR1_MA9	DDR1_DQ9	AL35	MDB9				
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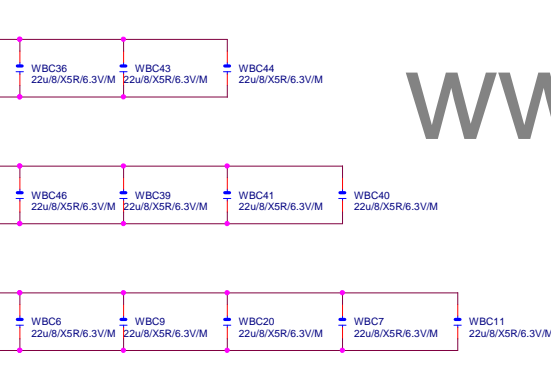
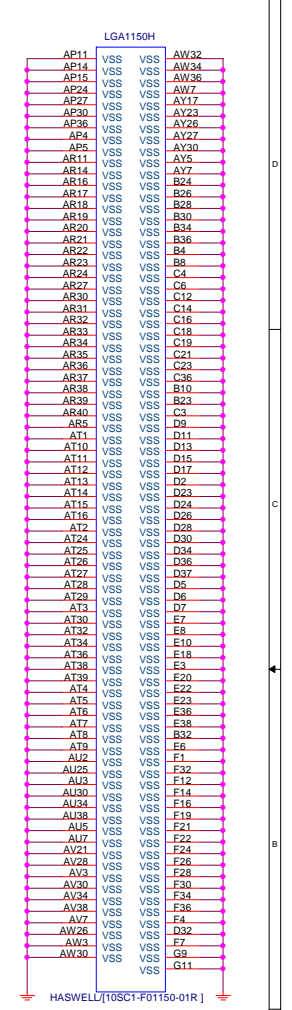
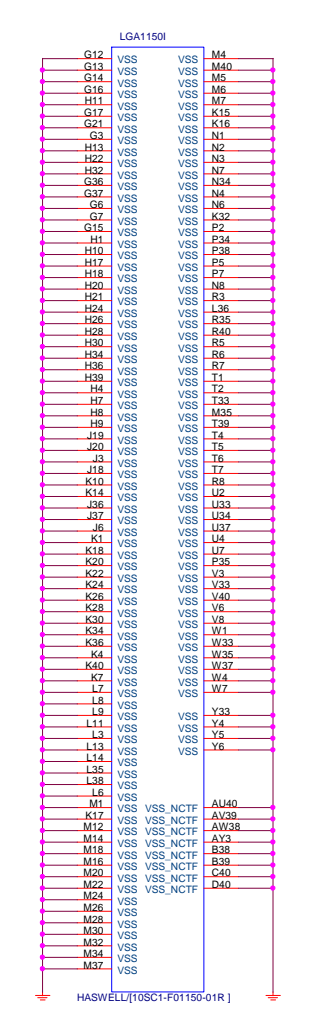
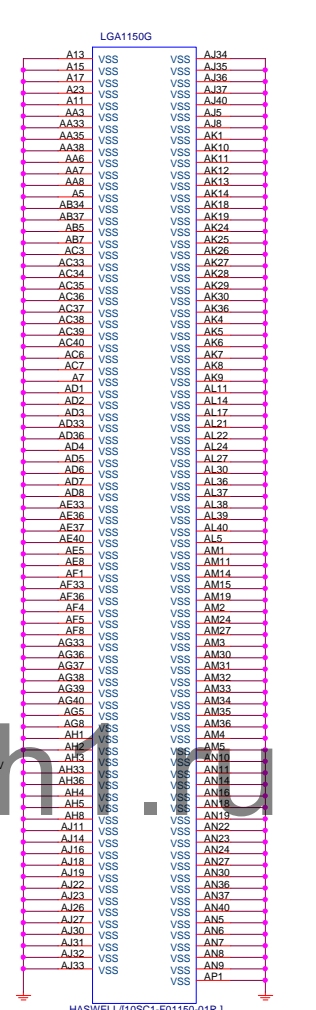
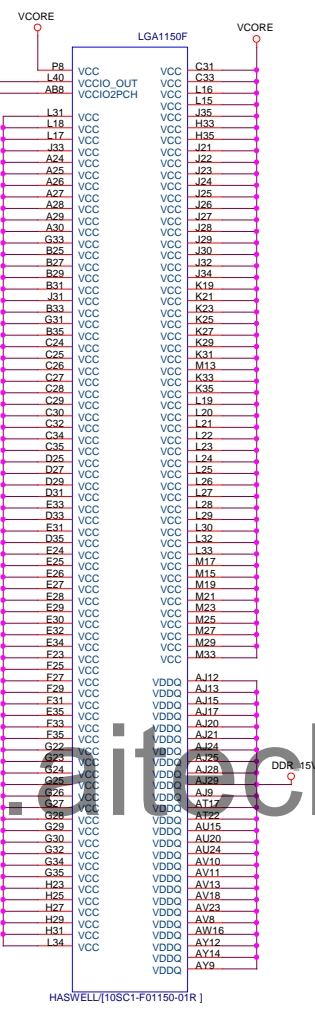
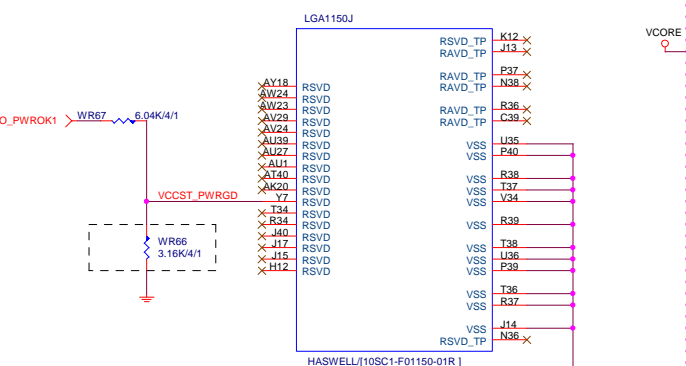
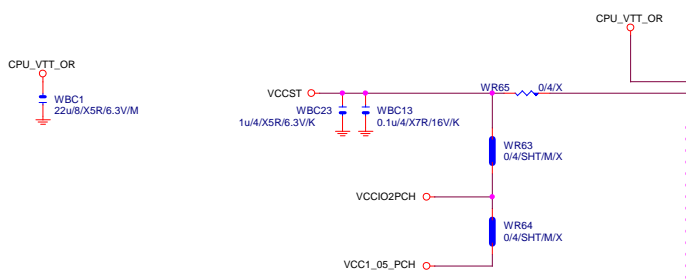


Need check the new CPU ME

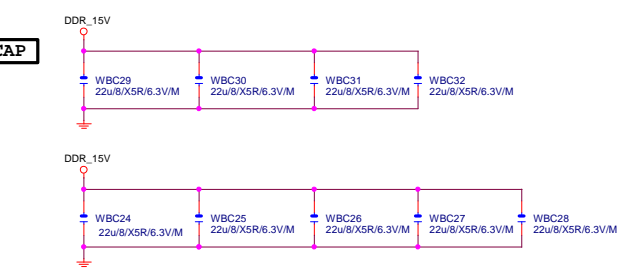


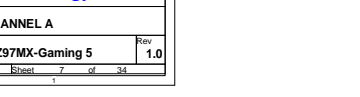
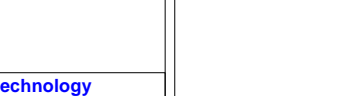
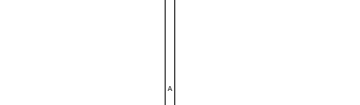
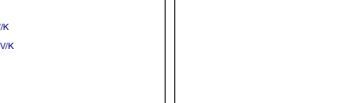
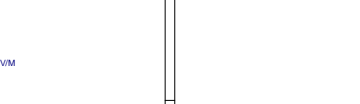
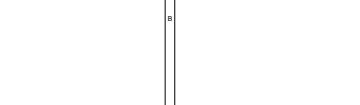
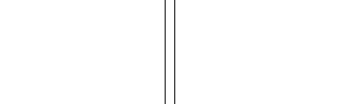
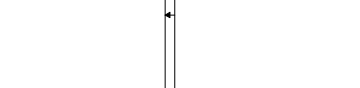
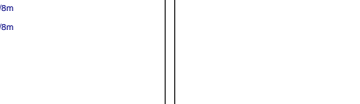
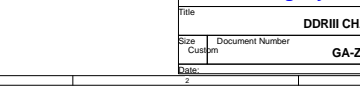
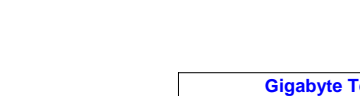
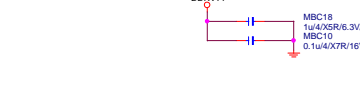
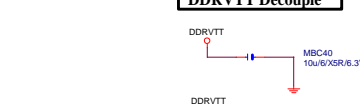
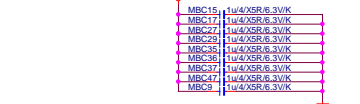
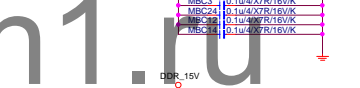
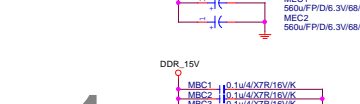
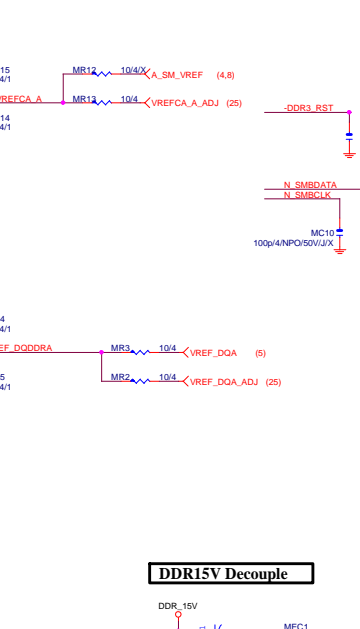
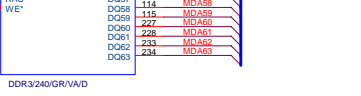
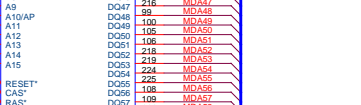
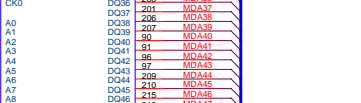
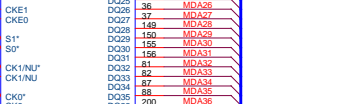
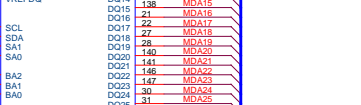
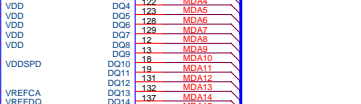
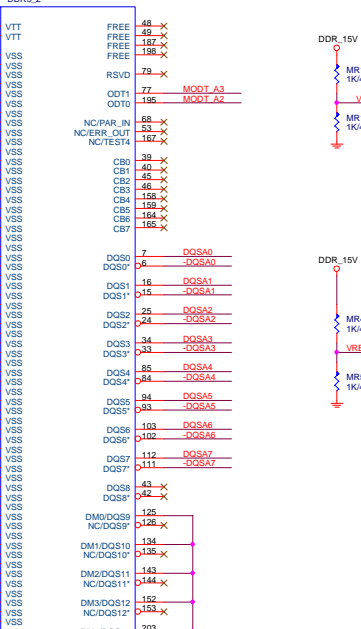
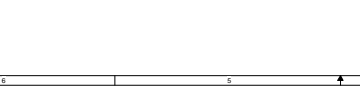
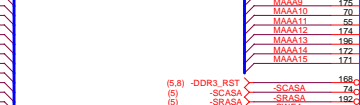
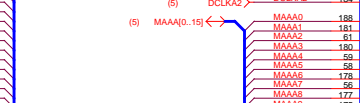
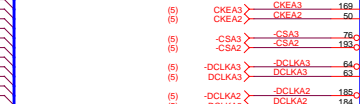
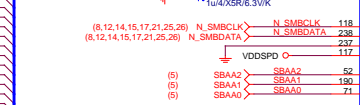
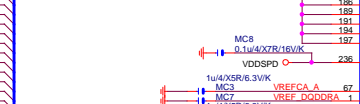
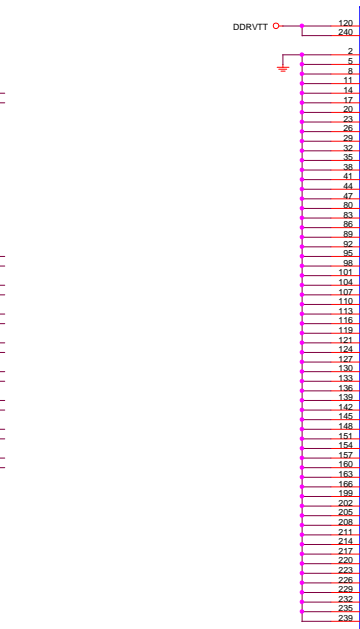
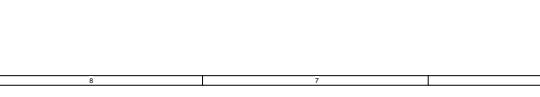
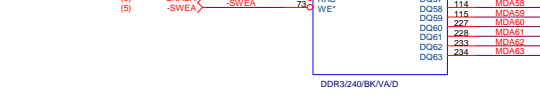
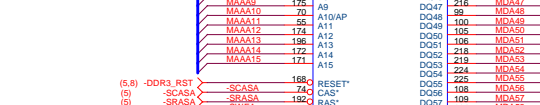
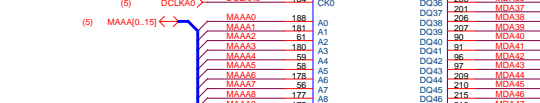
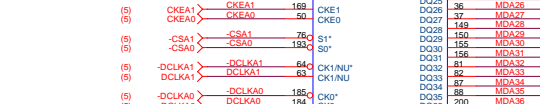
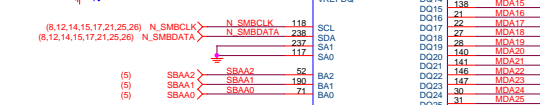
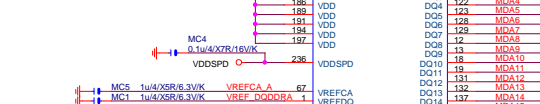
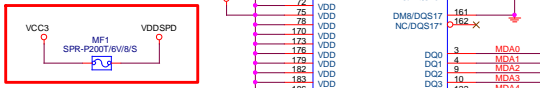
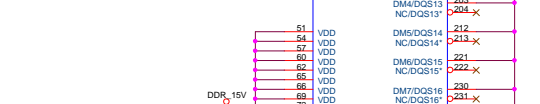
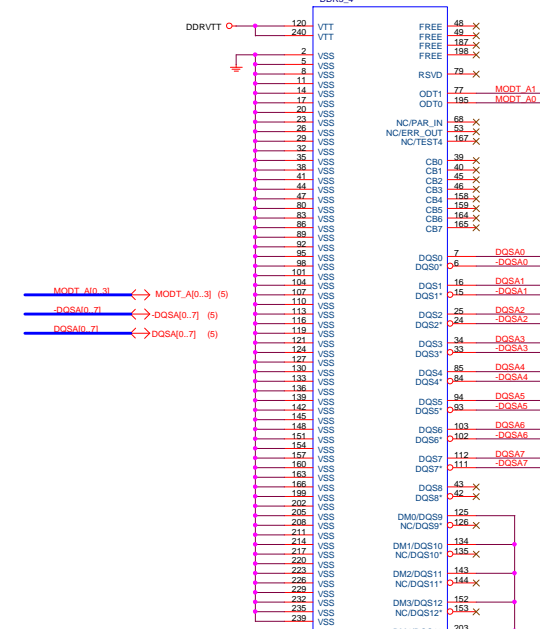
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- (7) MODT_A[0..3] <-- MODT_A[0..3]
- (8) MODT_B[0..3] <-- MODT_B[0..3]
- (7) MDA[0..63] <-- MDA[0..63]
- (8) MDB[0..63] <-- MDB[0..63]
- (7) DQSA[0..7] <-- DQSA[0..7]
- (7) -DQSA[0..7] <-- -DQSA[0..7]
- (7) MAAA[0..15] <-- MAAA[0..15]
- (8) MAAB[0..15] <-- MAAB[0..15]
- (8) DQSB[0..7] <-- DQSB[0..7]
- (8) -DQSB[0..7] <-- -DQSB[0..7]

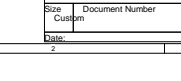
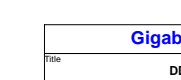
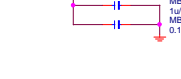
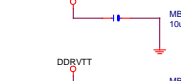
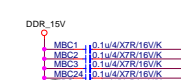
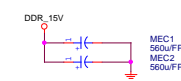


DDR CAP (X9)

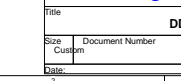
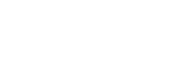
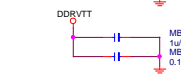
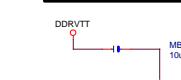




DDR15V Decouple

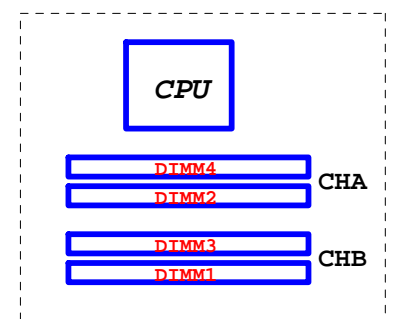
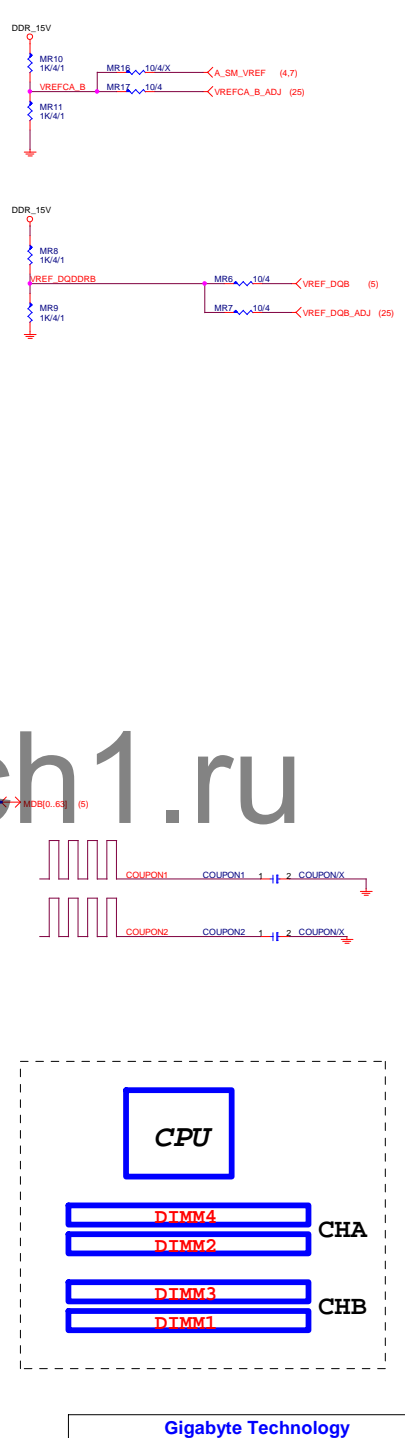
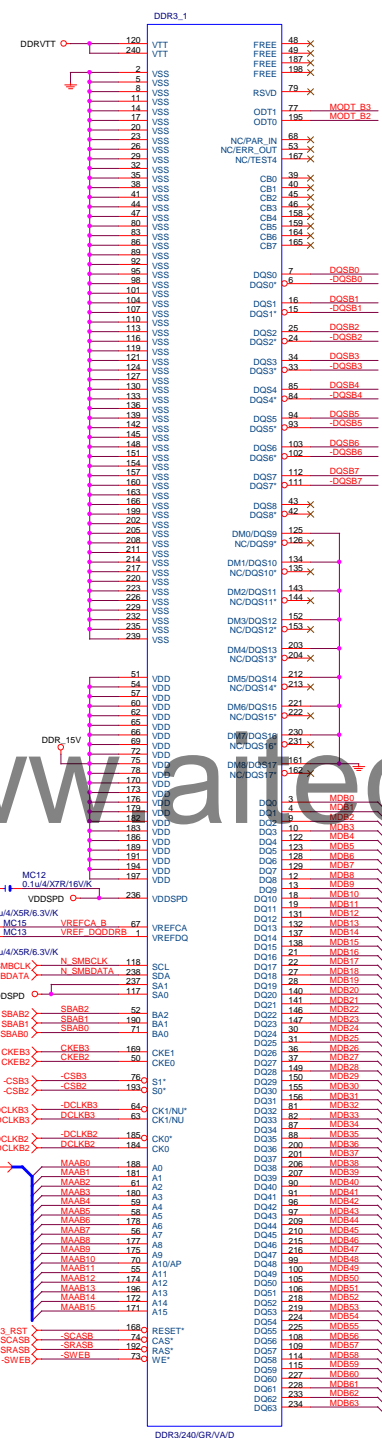
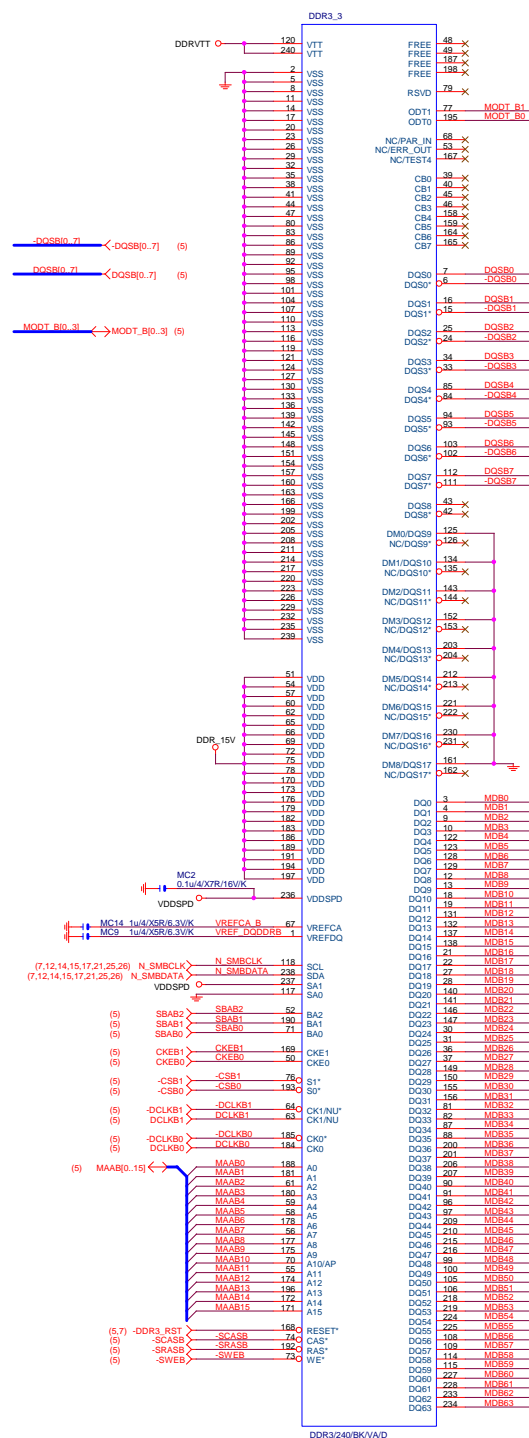


DDRVRTT Decouple



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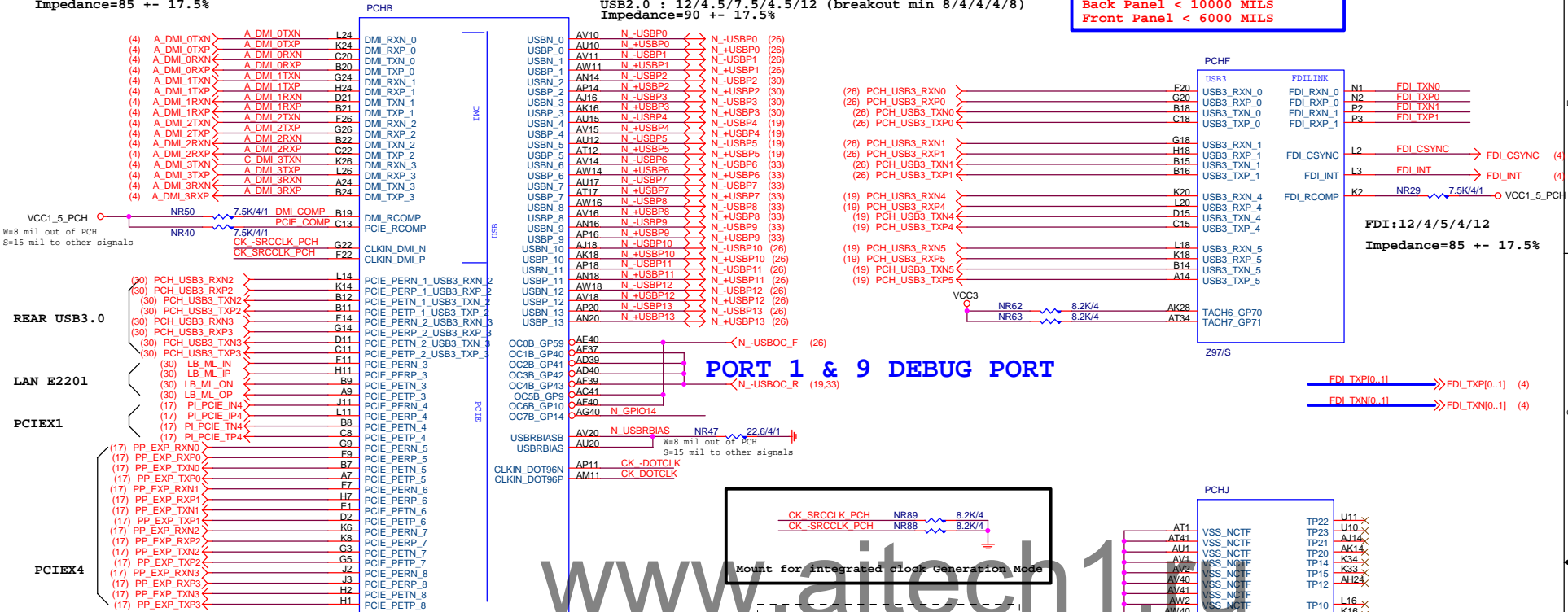
Title		DDRIII CHANNEL A	
Size		Document Number	
Custom		GA-Z97MX-Gaming 5	
Date		Rev	
		1.0	



DMI:12/4/4/12(breakout min 8/4/4/4/8)
Impedance=85 +- 17.5%

USB2.0 : 12/4/5/7/5/4/5/12 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%

USB3.0:20/5/7/5/20 (breakout min 8/4/4/4/8) ; ONLY 3 VIAS
Impedance=85 +- 17.5%
Back Panel < 10000 MILS
Front Panel < 6000 MILS

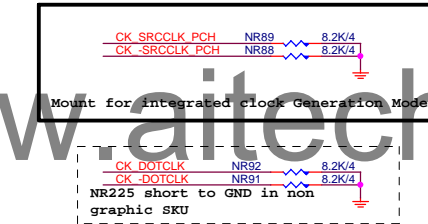


放靠近 Device & PCI-E Slot

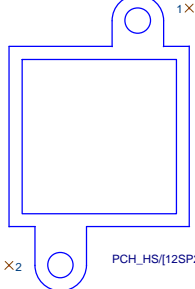
PCIEX1:16/5/5/16 (breakout min 8/4/4/4/8)

Impedance=80 +- 17.5%

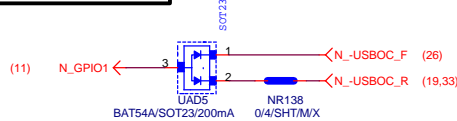
Z97/S
Must change to Z87 P/N
,before MP



PCH_HS



USB POWER PROTECT



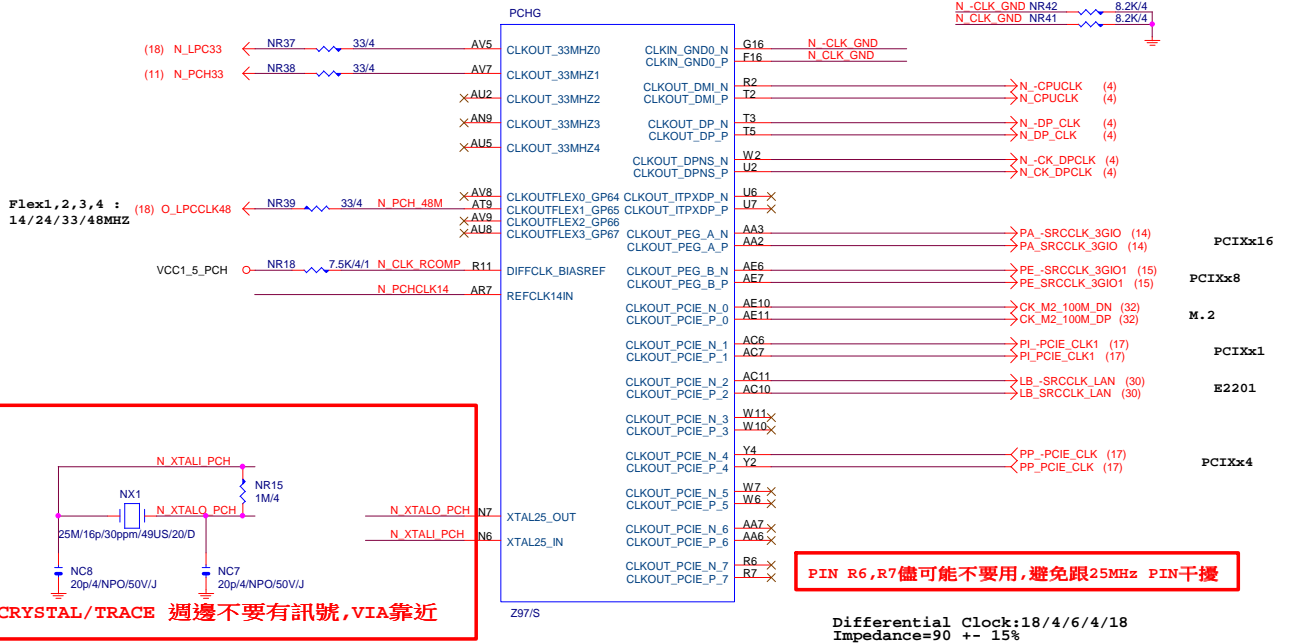
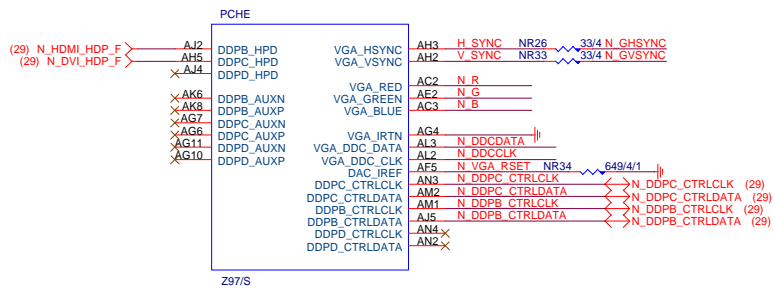
USB TABLE

OC[3:0]# for Device 29 (ports 0-7)
OC[7:4]# for Device 26 (ports 8-13)

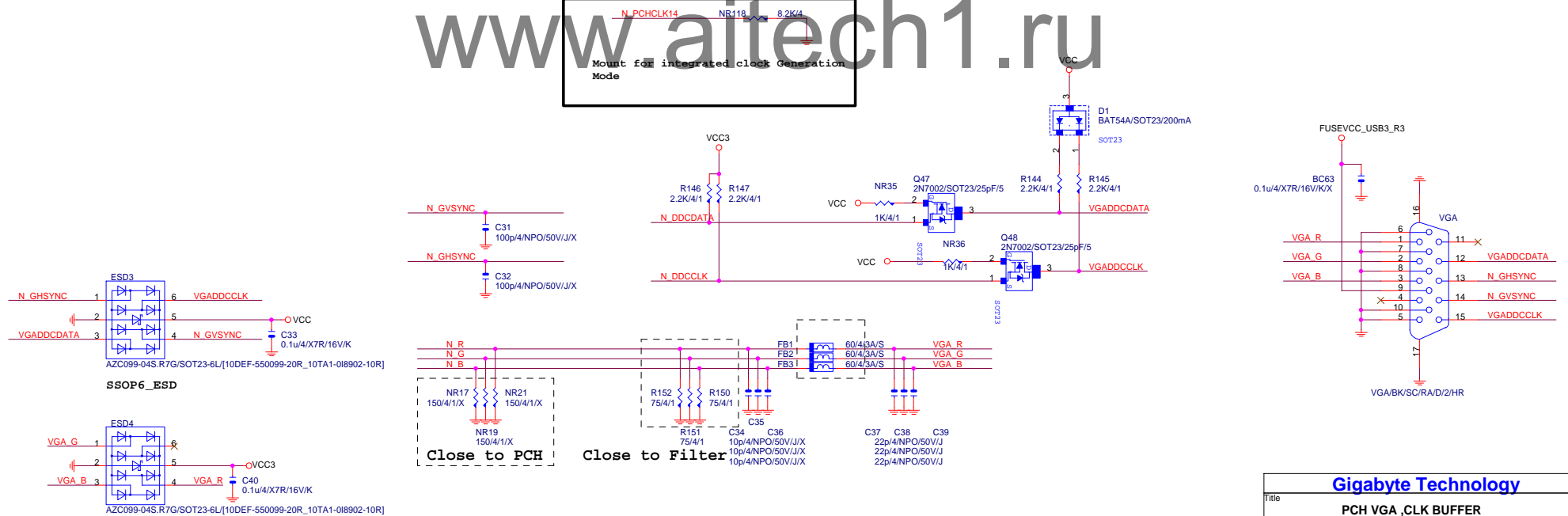
USB OC# Configure		
OC0#	USB0,1	F_USB30
OC1#	USB2,3	USB30_LAN
OC2#	USB4,5	R_USB30
OC3#	USB6,7	R_USB
OC4#	USB8,9	R_USB
OC5#	USB10,11	F_USB2
OC6#	USB12,13	F_USB
OC7#	Not Use	Not Use

Gigabyte Technology

Title		
PCH FDI,DMI,USB,PCIE		
Size	Document Number	Rev
Custom	GA-Z97MX-Gaming 5	1.0
Date:	Monday, May 12, 2014	Sheet 9 of 34

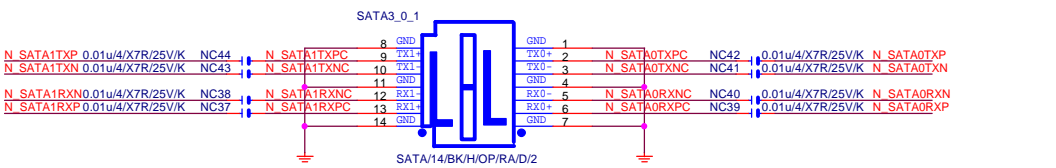
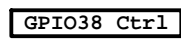


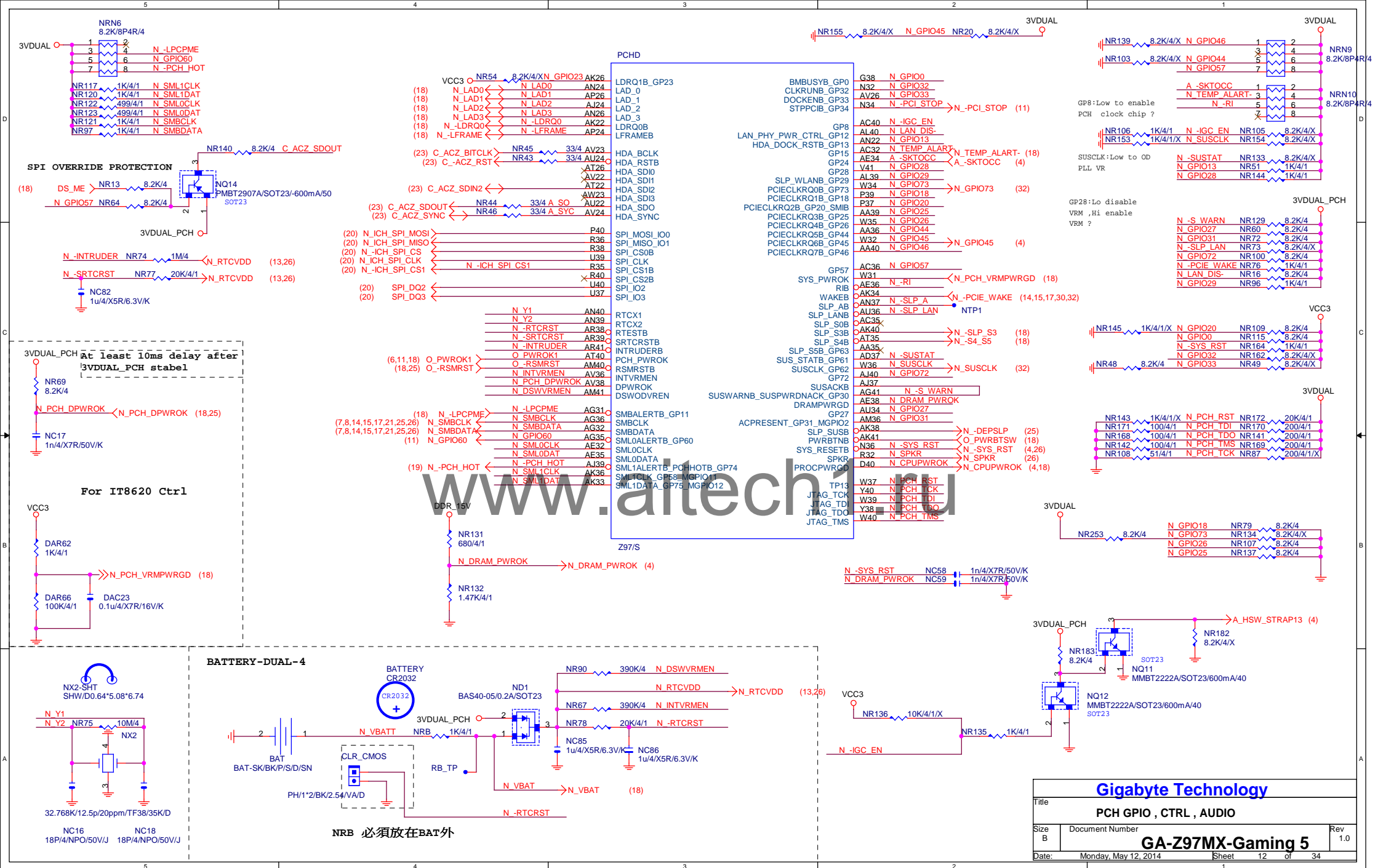
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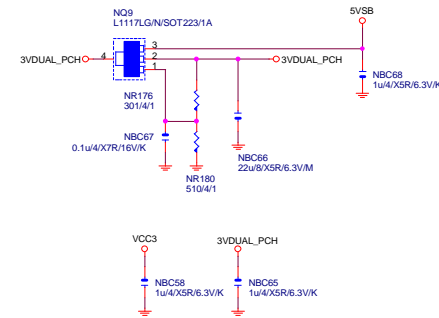
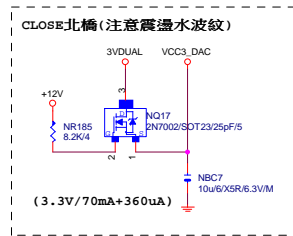


Gigabyte Technology			
Title			
PCH VGA ,CLK BUFFER			
Size	Document Number	Rev	
Custom	GA-Z97MX-Gaming 5		1.0
Date:	Monday, May 12, 2014	Sheet	10 of 34

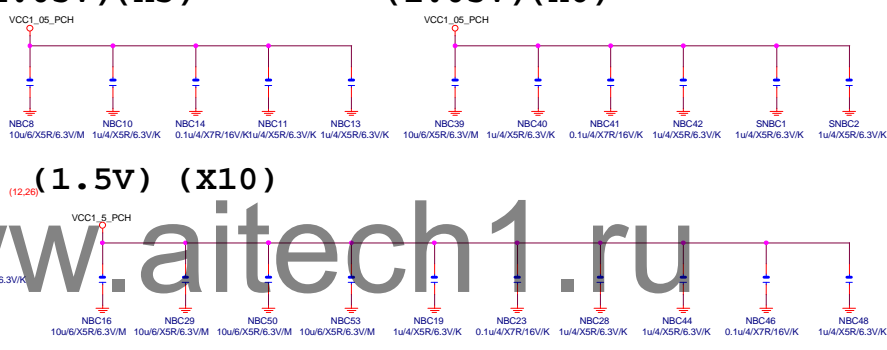
PCH						
36	CL_CLK	CLINK			SATA_RXN_0	
37	CL_DATA				SATA_RXP_0	
34	CL_RSTB				SATA_TXN_0	
32	APWROK				SATA_TXP_0	
					SATA_RXN_1	
					SATA_RXP_1	
					SATA_TXN_1	
					SATA_TXP_1	
		F2M			SATA_RXN_2	
31	PWM0				SATA_RXP_2	
31	PWM1				SATA_TXN_2	
30	PWM2				SATA_TXP_2	
	PWM3				SATA_RXN_3	
					SATA_RXP_3	
28	TACH0_GP17				SATA_TXN_3	
31	TACH1_GP1				SATA_TXP_3	
28	TACH2_GP6					
34	TACH3_GP7			SATA_RXN_4_PCIE_PERN_1		
30	SDATA4_GP68			SATA_RXP_4_PCIE_PERP_1		
35	TACH5_GP69			SATA_TXN_4_PCIE_PETN_1		
				SATA_TXP_4_PCIE_PETP_1		
31	SSTCTL			SATA_RXN_5_PCIE_PERN_2		
				SATA_RXP_5_PCIE_PERP_2		
38	SCLOCK_GP22			SATA_TXN_5_PCIE_PETN_2		
41	SLOAD_GP38			SATA_TXP_5_PCIE_PETP_2		
31	SDATAOUT0_GP39			CLKIN_SATA_N		
40	SDATAOUT1_GP48			CLKIN_SATA_P		
		GPIO			SATALED0B	
						SATA_RCOMP
					SATA0GP_GP21	
					SATA1GP_GP19	
				SATA2GP_GP36		
				SATA3GP_GP37		
				SATA4GP_GP16		
				SATA5GP_GP49		
				EDP_BKLCTCL		
				EDP_BKLTEN		
				EDP_VDDEN		
		HOST			RSVD	
					RCINB	
					SERIRQ	
					THRMTTRIPB	
				PECI		
				PM_SYNCN		
				PLTRST_PROCB		







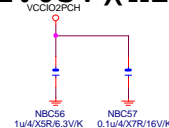
(1.05V) (x6)



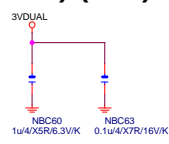
(1.5V) (x10)

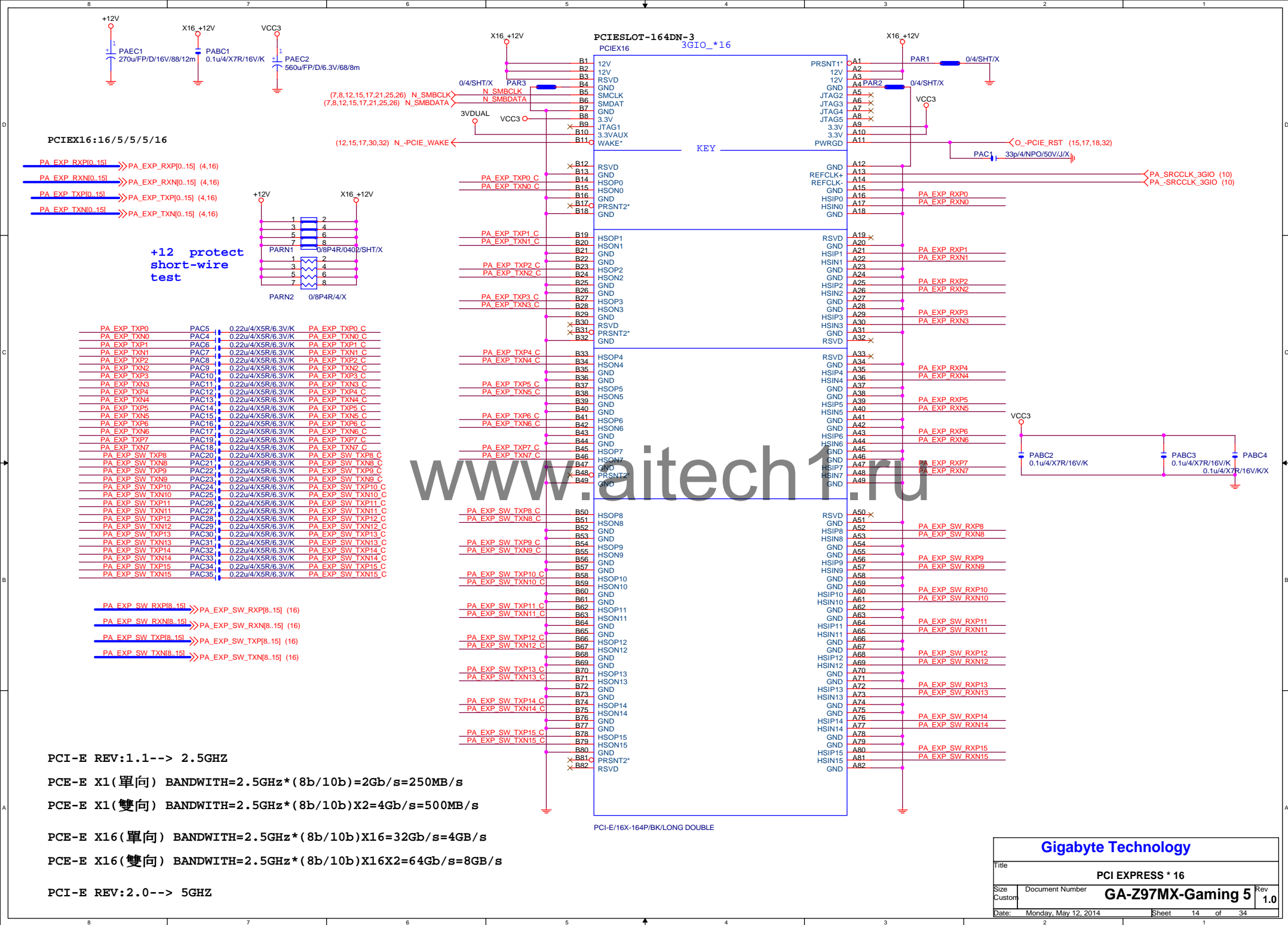


(1.05V)(x2)



(3.3V) (X2)

[illegible]



PCIEX16:16/5/5/16

PA EXP RXP0.15] >> PA_EXP_RXP0[.15] (4,16)
PA EXP RXN0.15] >> PA_EXP_RXN0[.15] (4,16)
PA EXP TXP0.15] >> PA_EXP_TXP0[.15] (4,16)
PA EXP TXN0.15] >> PA_EXP_TXN0[.15] (4,16)

+12 protect
short-wire
test

PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

PA EXP SW RXP8.15] >> PA_EXP_SW_RXP8[.15] (16)
PA EXP SW RXN8.15] >> PA_EXP_SW_RXN8[.15] (16)
PA EXP SW TXP8.15] >> PA_EXP_SW_TXP8[.15] (16)
PA EXP SW TXN8.15] >> PA_EXP_SW_TXN8[.15] (16)

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

Gigabyte Technology

Title

PCI EXPRESS * 16

Size Custom

Document Number

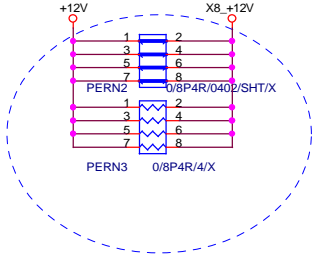
GA-Z97MX-Gaming 5

Date: Monday, May 12, 2014

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Rev 1.0

+12 protect
short-wire
test



(7,8,12,14,17,21,25,26) N_SMBCLK PER3
(7,8,12,14,17,21,25,26) N_SMBDATA PER5

(12,14,17,30,32) N_PCIE_WAKE

PE_EXP_SW_TXP8_C
PE_EXP_SW_TXN8_C

PE_EXP_SW_TXP9_C
PE_EXP_SW_TXN9_C

PE_EXP_SW_TXP10_C
PE_EXP_SW_TXN10_C

PE_EXP_SW_TXP11_C
PE_EXP_SW_TXN11_C

PE_EXP_SW_TXP12_C
PE_EXP_SW_TXN12_C

PE_EXP_SW_TXP13_C
PE_EXP_SW_TXN13_C

PE_EXP_SW_TXP14_C
PE_EXP_SW_TXN14_C

PE_EXP_SW_TXP15_C
PE_EXP_SW_TXN15_C

PE_EXP_SW_TXP8_C	PEC2	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP8_C
PE_EXP_SW_TXN8_C	PEC3	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN8_C
PE_EXP_SW_TXP9_C	PEC4	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP9_C
PE_EXP_SW_TXN9_C	PEC5	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN9_C
PE_EXP_SW_TXP10_C	PEC6	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP10_C
PE_EXP_SW_TXN10_C	PEC7	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN10_C
PE_EXP_SW_TXP11_C	PEC8	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP11_C
PE_EXP_SW_TXN11_C	PEC9	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN11_C
PE_EXP_SW_TXP12_C	PEC10	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP12_C
PE_EXP_SW_TXN12_C	PEC11	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN12_C
PE_EXP_SW_TXP13_C	PEC12	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP13_C
PE_EXP_SW_TXN13_C	PEC13	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN13_C
PE_EXP_SW_TXP14_C	PEC14	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP14_C
PE_EXP_SW_TXN14_C	PEC15	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN14_C
PE_EXP_SW_TXP15_C	PEC16	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXP15_C
PE_EXP_SW_TXN15_C	PEC17	0.22u/4/X5R/6.3V/K	PE_EXP_SW_TXN15_C

(16) PE_16_8_SW

(4) -8X_EN

PED1
BAT54C/SOT23/200mA

VCC3
PER6
8.2K/4/X

(11) N_GPIO39

PCI-E/8X-99P/BK/LONG DOUBLE

3GIO_*8

KEY

X8_+12V

VCC3

PER1
0/4/SHT/X

O_PCIE_RST (14,17,18,32)
PEC1
22p/4/NPO/50V/J/X

PE_SRCCLK_3GIO1 (10)
PE_SRCCLK_3GIO1 (10)

PE_EXP_SW_RXP8
PE_EXP_SW_RXN8

PE_EXP_SW_RXP9
PE_EXP_SW_RXN9

PE_EXP_SW_RXP10
PE_EXP_SW_RXN10

PE_EXP_SW_RXP11
PE_EXP_SW_RXN11

PE_EXP_SW_RXP12
PE_EXP_SW_RXN12

PE_EXP_SW_RXP13
PE_EXP_SW_RXN13

PE_EXP_SW_RXP14
PE_EXP_SW_RXN14

PE_EXP_SW_RXP15
PE_EXP_SW_RXN15

PE_EXP_SW_RXP15] >>> PE_EXP_SW_RXP[8.15] (16)

PE_EXP_SW_RXN15] >>> PE_EXP_SW_RXN[8.15] (16)

PE_EXP_SW_TXP[8.15] >>> PE_EXP_SW_TXP[8.15] (16)

PE_EXP_SW_TXN[8.15] >>> PE_EXP_SW_TXN[8.15] (16)

3VDUAL

PEBC3
1u/4/X5R/6.3V/K

+12V

PEBC1
0.1u/4/X7R/16V/K

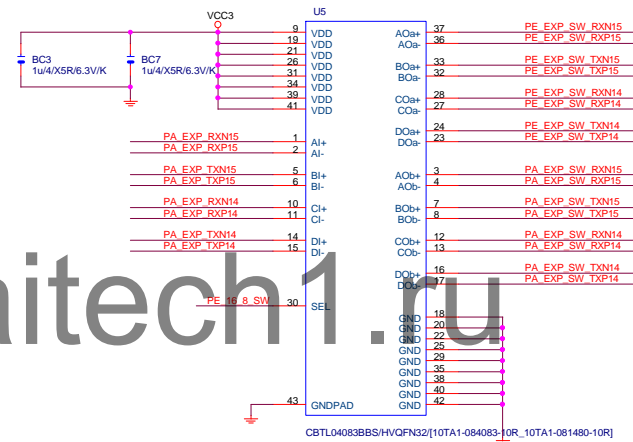
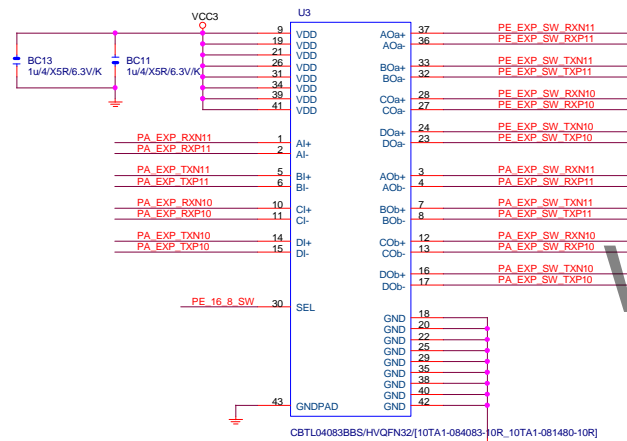
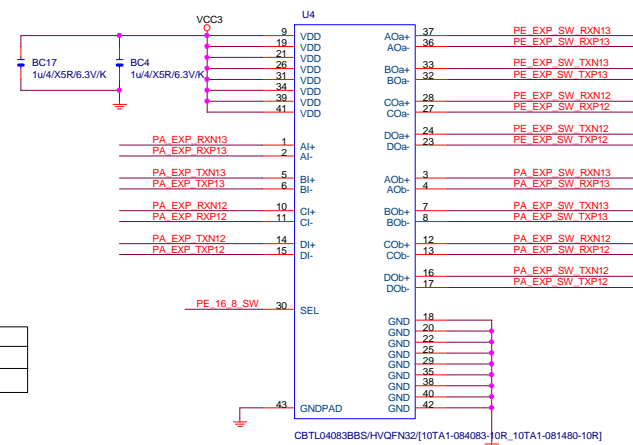
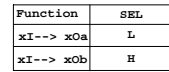
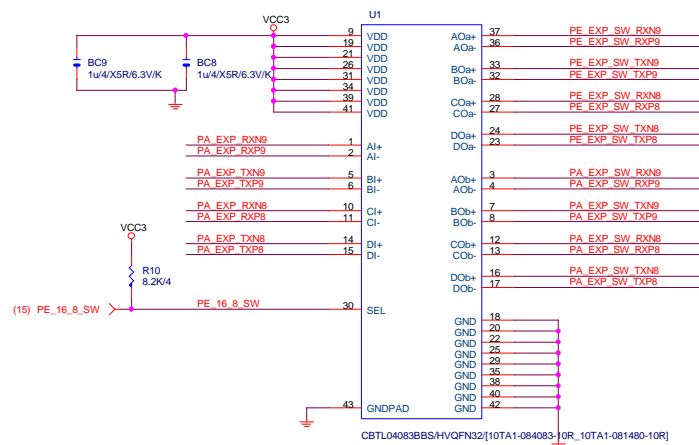
VCC3

PEBC2
0.1u/4/X7R/16V/K

PEBC4
0.1u/4/X7R/16V/K/X

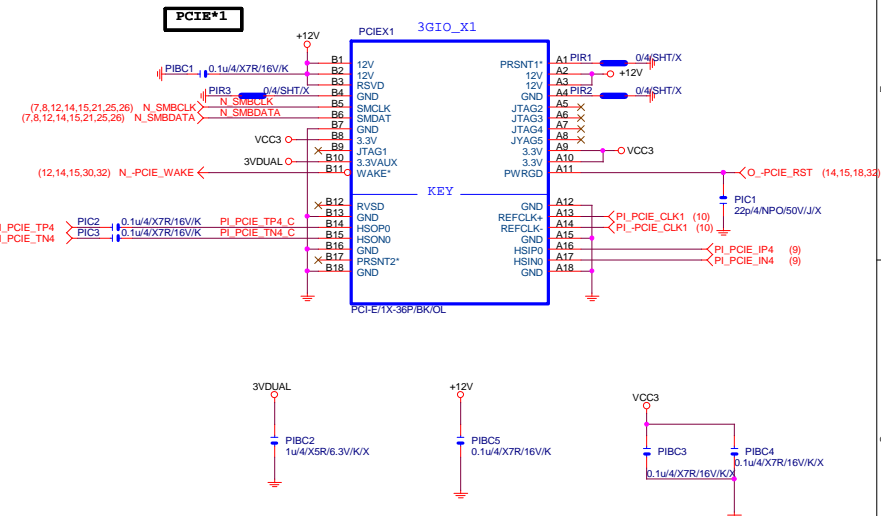
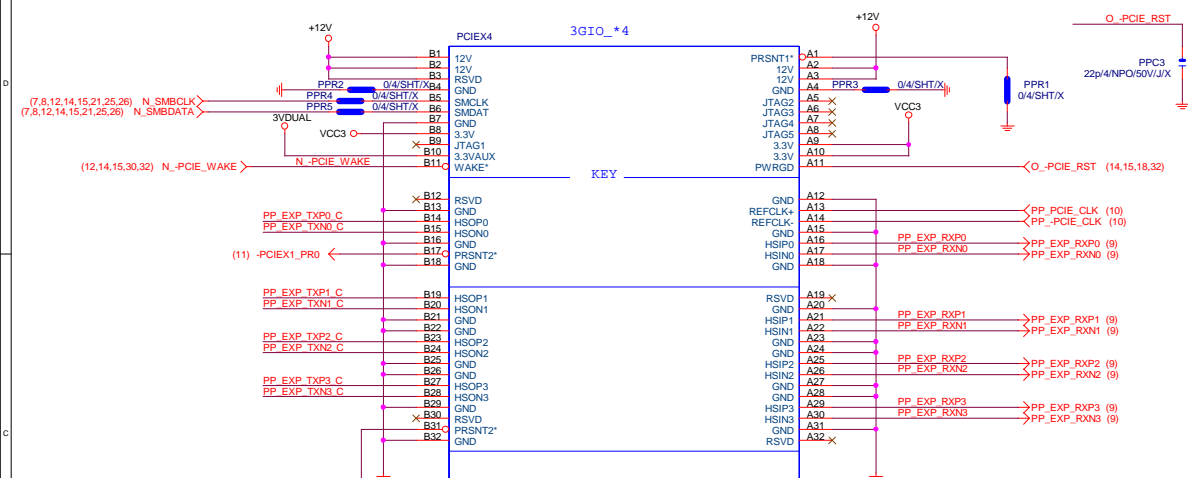
Gigabyte Technology

Title			PCI EXPRESS X 8 PORT	
Size	Document Number	GA-Z97MX-Gaming 5		Rev
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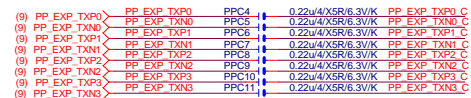
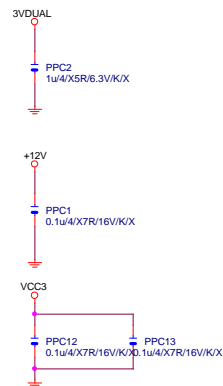


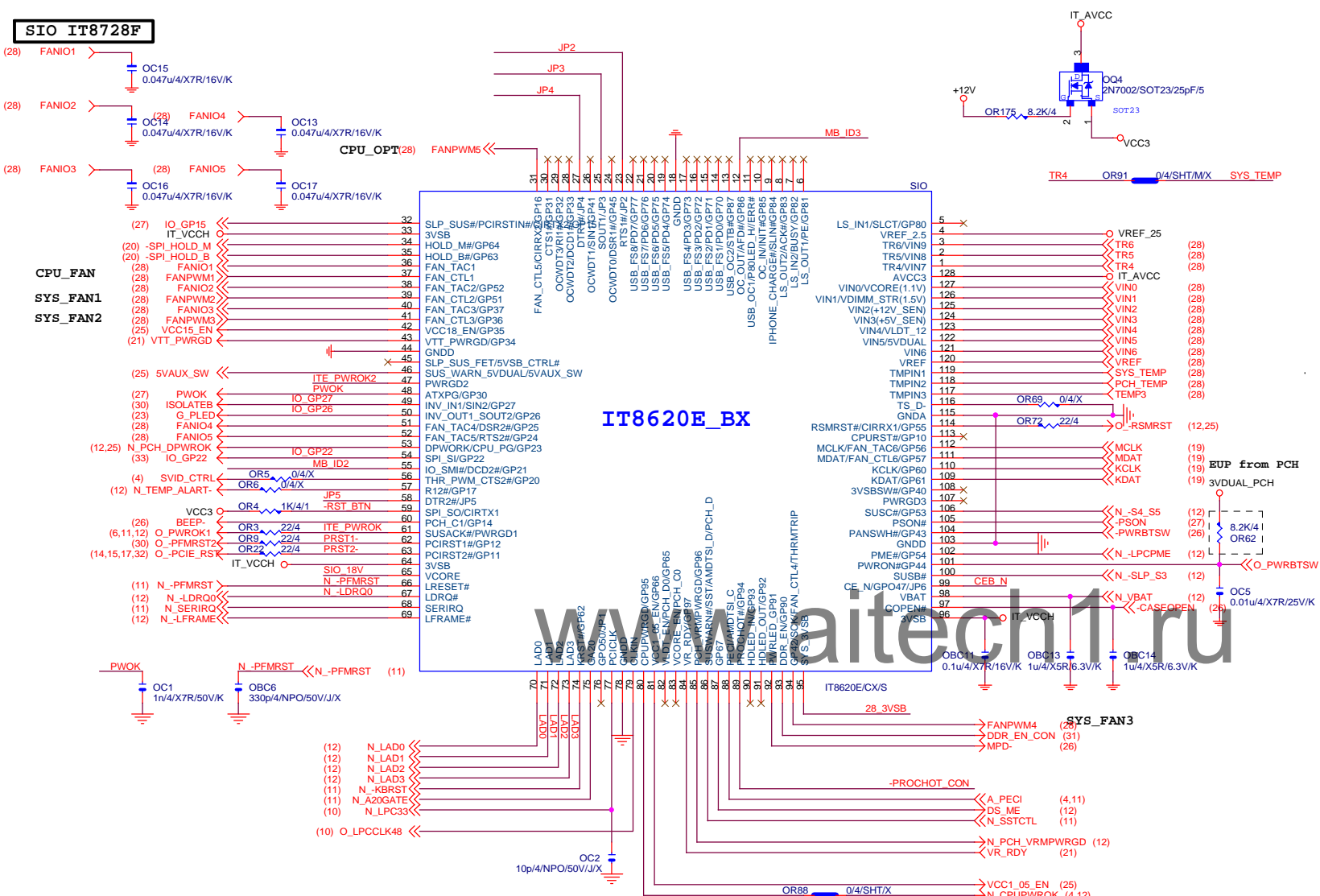
<u>PA_EXP_RXP[0..15]</u>	⇒ PA_EXP_RXP[0..15] (4,14)
<u>PA_EXP_RXN[0..15]</u>	⇒ PA_EXP_RXN[0..15] (4,14)
<u>PA_EXP_TXP[0..15]</u>	⇒ PA_EXP_TXP[0..15] (4,14)
<u>PA_EXP_TXN[0..15]</u>	⇒ PA_EXP_TXN[0..15] (4,14)
<u>PA_EXP_SW_RXP[8..15]</u>	⇒ PA_EXP_SW_RXP[8..15] (14)
<u>PA_EXP_SW_RXN[8..15]</u>	⇒ PA_EXP_SW_RXN[8..15] (14)
<u>PA_EXP_SW_TXP[8..15]</u>	⇒ PA_EXP_SW_TXP[8..15] (14)
<u>PA_EXP_SW_TXN[8..15]</u>	⇒ PA_EXP_SW_TXN[8..15] (14)
<u>PE_EXP_SW_RXP[8..15]</u>	⇒ PE_EXP_SW_RXP[8..15] (15)
<u>PE_EXP_SW_RXN[8..15]</u>	⇒ PE_EXP_SW_RXN[8..15] (15)
<u>PE_EXP_SW_TXP[8..15]</u>	⇒ PE_EXP_SW_TXP[8..15] (15)
<u>PE_EXP_SW_TXN[8..15]</u>	⇒ PE_EXP_SW_TXN[8..15] (15)

PCIE*4

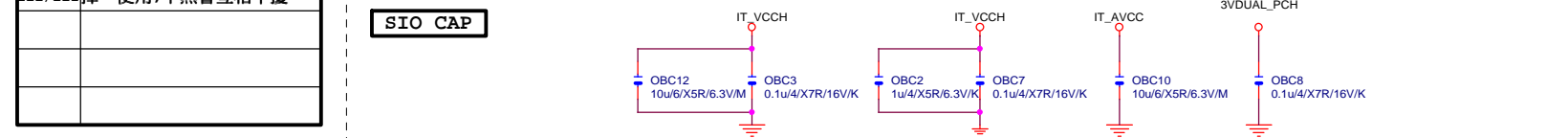
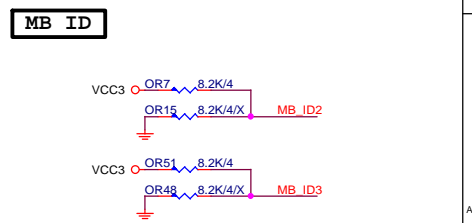
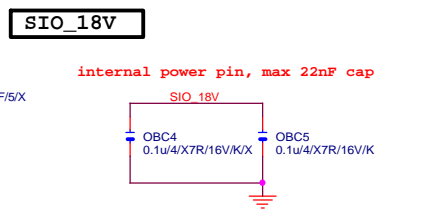
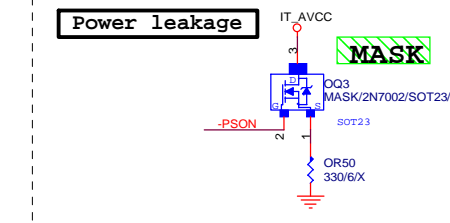
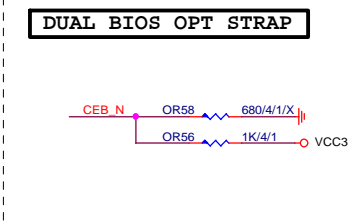


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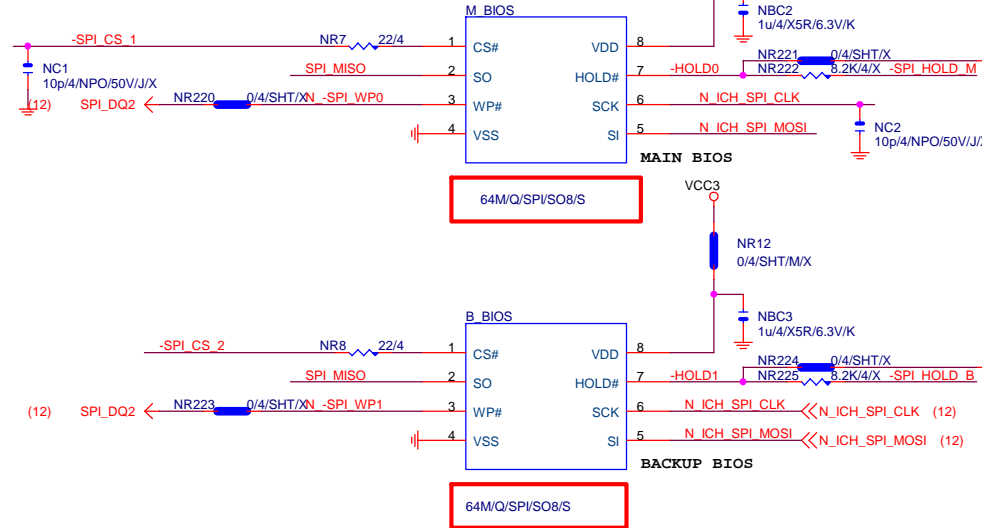
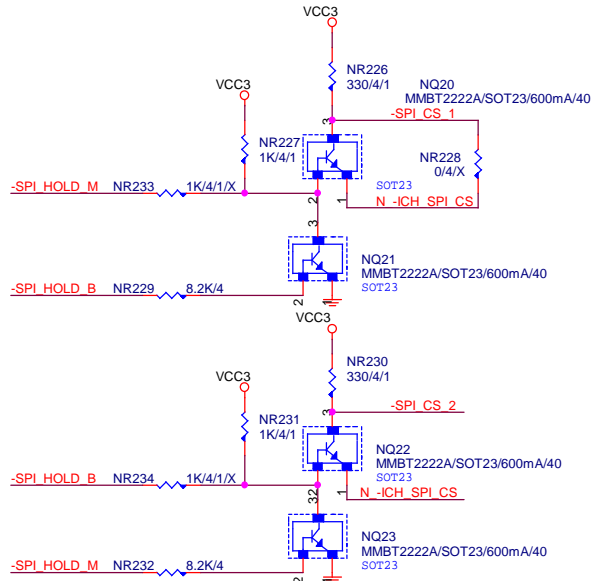


IT8620E GPIO問題匯整	
PIN 50	GP26--- 第一次接上POWER時會拉 LO
PIN 90/91	DEFAULT為HDLLED FUNCTION, GP93 BYPASS TO GP92 高溫時 GP92 會被拉Lo(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 LO
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用, 不然會互相干擾

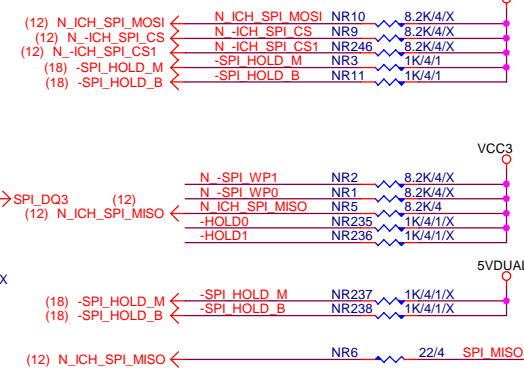


Gigabyte Technology	
Title	
ITE 8620 LPC IO	
Size B	Document Number
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DUAL BIOS



MOSI For DMI RX Termination Voltage

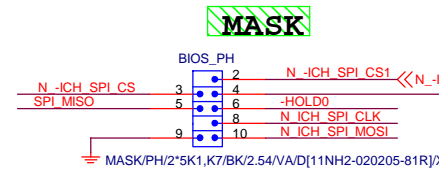


BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

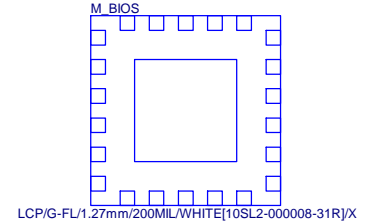
1 means floating
0 means PD 1K

TPM CONNECT

BIOS Debug port



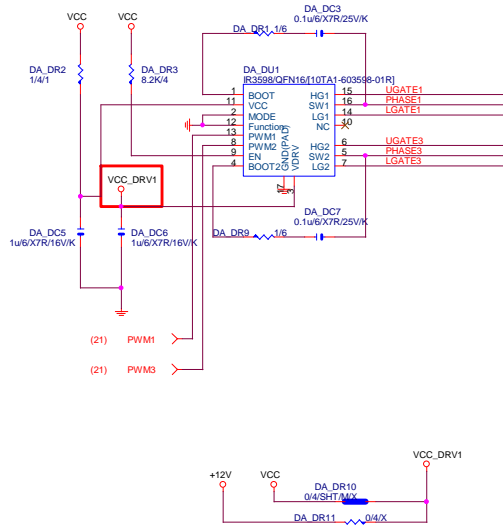
PVT要改MASK



Gigabyte Technology

Title		BIOS & TPM	
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Custom			
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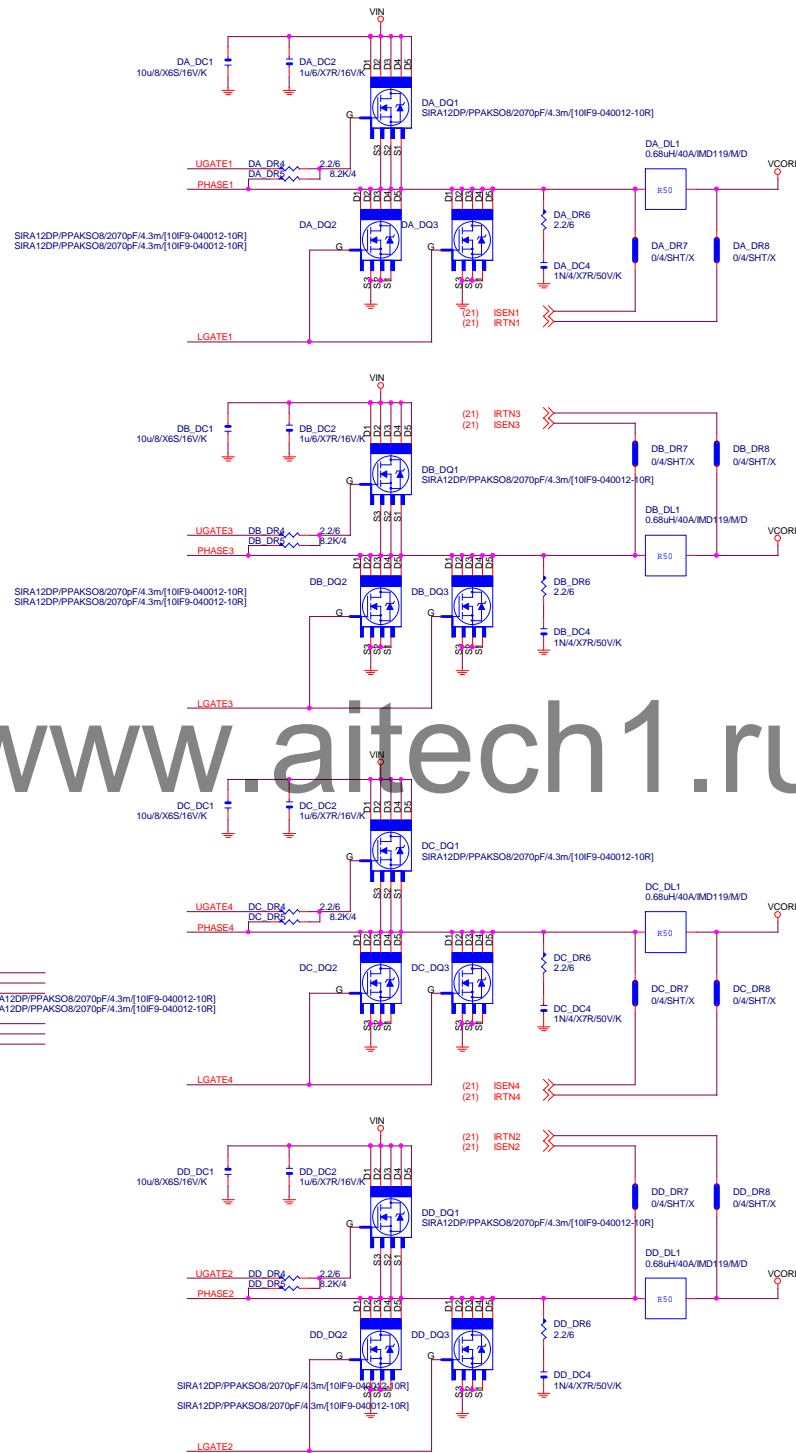
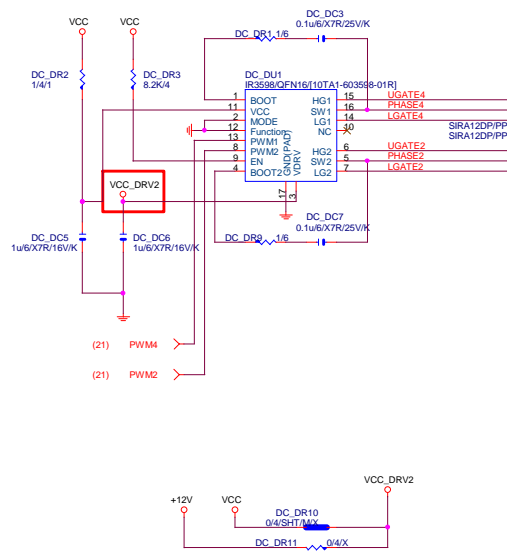
VCORE Phase 1,3



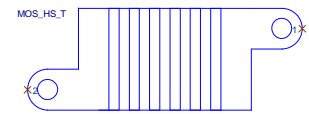
FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	18 ATX	DUAL
1	1	18 ATX	Doubler
0	0	Tri-State	DUAL
1	0	Tri-State	Doubler
OPEN	0	Tri-State	Quad
OPEN	1	18 ATX	Quad

In Quad mode, IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

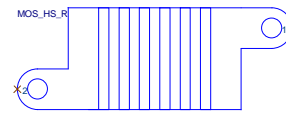
VCORE Phase 4,2



MOSFET HEATSINK



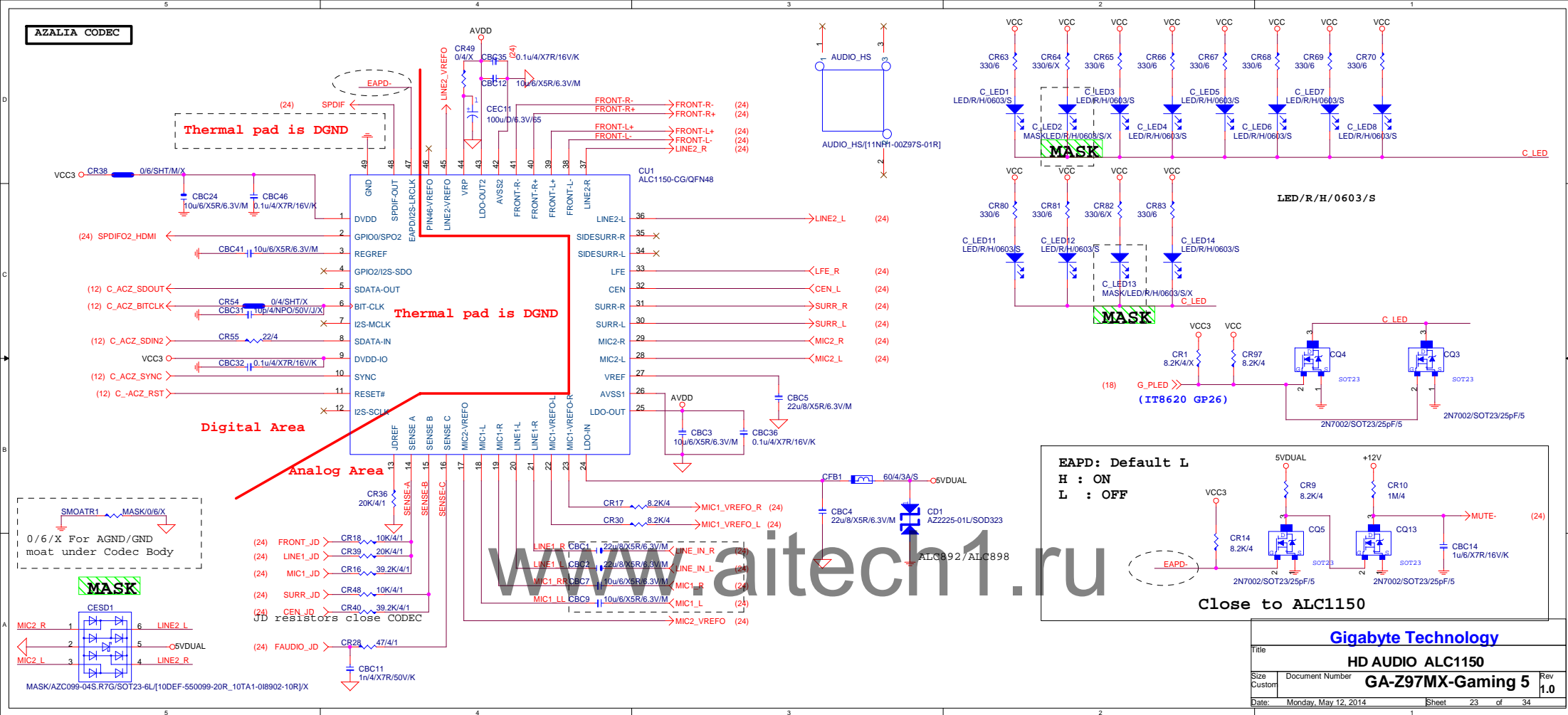
MOS_HeatSink[12SP2-S07924-01R_12SP2-S07924-02R_12SP2-S07924-03R]



MOS_HeatSink[12SP2-S07924-21R_12SP2-S07924-22R_12SP2-S07924-23R]

Gigabyte Technology

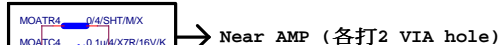
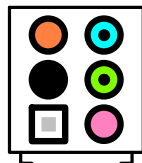
Title	CPU CORE VR
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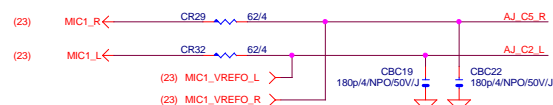
Gigabyte Technology

HD AUDIO ALC1150

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MIC-IN



(23) SPDIF02_HDMI

CR52

0/4/SHTM/X

100pF

CBC37

SPDIF_O

PH/1'2/BK/2.54V/A/D

1~4	GAIN
OFF	X2.5
ON	X6

OFF X2.5
ON X6

AMP SLOT1[11SI-010204-12R]

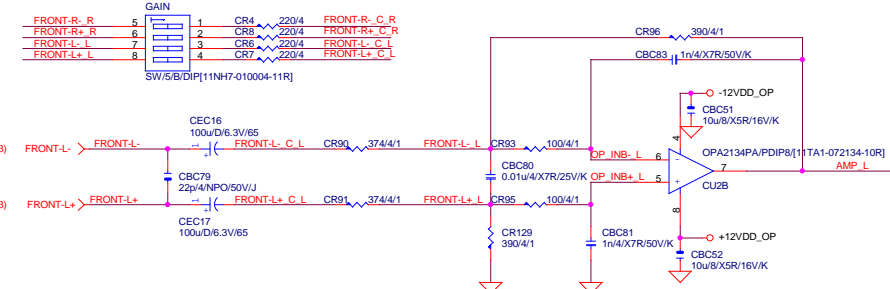
(23) FRONT-R- > FRONT-R- \rightarrow CEC14 100u/D16.3V/65 \rightarrow FRONT-R- C R CR73 374u/4/1 FRONT-R- R CR76 100u/4/1
 CBC76 22p/4/INPO/50V/J
 (23) FRONT-R+ > FRONT-R+ \rightarrow FRONT-R+ C R CR74 374u/4/1 FRONT-R+ R CR78 100u/4/1
 CEC15 100u/D16.3V/65

OP INA- R 2
 OP INA+ R 3
 OP 1
 CBC82 1n4/X7R/50V/K
 CR79 390u/4/1
 CBC81 1n4/X7R/50V/K
 CEC49 0.1u/4/X7R/16V/K
 CEC50 0.1u/4/X7R/16V/K
 CBC87 1n4/X7R/50V/K
 CR128 390u/4/1
 CEC77 0.01u/4/X7R/25V/K
 CEC78 100u/4/1
 CEC79 390u/4/1
 CEC80 100u/4/1
 CEC81 100u/4/1
 CEC82 100u/4/1
 CEC83 100u/4/1
 CEC84 100u/4/1
 CEC85 100u/4/1
 CEC86 100u/4/1
 CEC87 100u/4/1
 CEC88 100u/4/1
 CEC89 100u/4/1
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 CEC92 100u/4/1
 CEC93 100u/4/1
 CEC94 100u/4/1
 CEC95 100u/4/1
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 CEC98 100u/4/1
 CEC99 100u/4/1
 CEC100 100u/4/1

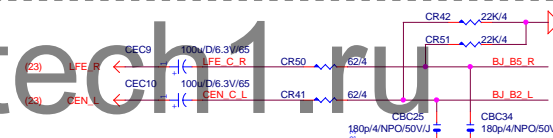
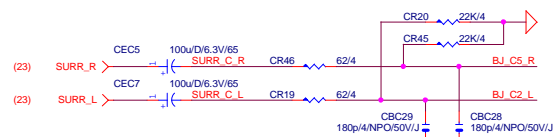
-12VDD_OP
 +12VDD_OP

OPA2134PA/PDIP8[11TA-072134-10R]
 AMP_R

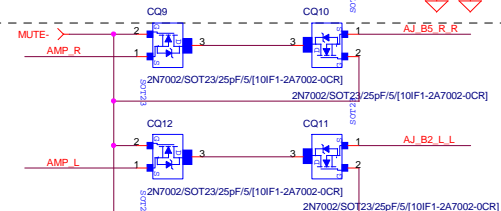
放大倍率： $V_{OUT} = (R_2 / (V_+ - V_-)) \cdot R_1$



CEN/LFE



SURR BACK



AZALIA JACK

Blue
LINE-IN

Green
LINE-OUT

Pink
MIC-IN

Orange
CEN/LFE

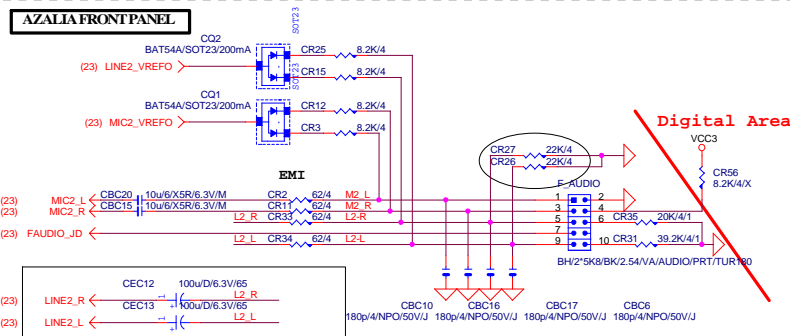
Black
SURROUND

SPDIF

OPTICAL

2X3RP/26P/BK GY BU GE PK/RA[11NR6-403025-81R]

2X3RP/26P/BK GY BU GE PK/RA[11NR6-403025-81R]



\\ Digital Area

Gigabyte Technology

AUDIO JACK

GA-Z97MX-Gaming 5

Rev	1.0
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Title

9

Size
Custo

Custo

Document Number

[illegible]

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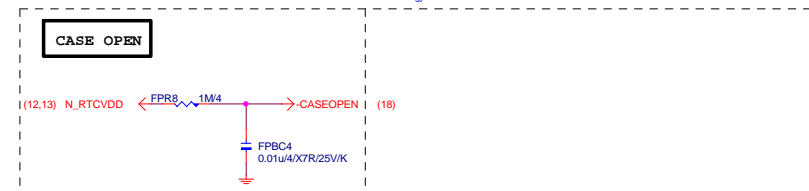
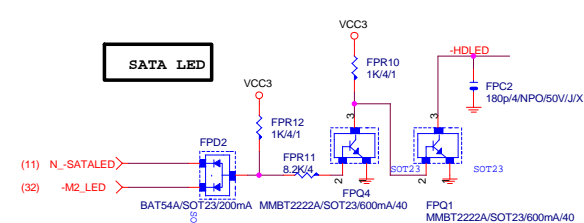
[illegible]

Figure 1: USB2.0/3.0 connector pinout. The diagram shows a USB connector with pins 1 through 10. Pins 1 and 2 are connected to FUSEVCC_F2 and FUSEVCC_F2 respectively. Pins 3 and 4 are connected to UBC1 and UBC2 respectively. Pins 5 and 6 are connected to N_USB12 and N_USB13 respectively. Pins 7 and 8 are connected to N_USB12 and N_USB13 respectively. Pins 9 and 10 are connected to N_USB12 and N_USB13 respectively. The connector is labeled BH2'5K9BK/ON2.54N/A/USB/PRT/7UR180. Below the connector is a schematic of the ESD6 diode array, showing connections for N_USB12, N_USB13, and 3VDUAL.

The circuit diagram shows a buzzer driver stage. It includes two NPN transistors, Q28 (2N7002) and Q29 (MMBT2222), both configured as common-emitter amplifiers. The input signal, labeled "BEEP" and "(18)", is connected to the base of Q28 through a resistor R178 (8.2K). The emitter of Q28 is grounded. The collector of Q28 is connected to the base of Q29 through a resistor R179 (1K/4/1). The emitter of Q29 is grounded. The collector of Q29 is connected to the positive terminal of a buzzer, represented by a speaker symbol. The negative terminal of the buzzer is connected to ground. A feedback path is shown from the output of the buzzer back to the input of Q28 through a resistor R180 (8.2K/4). The entire circuit is powered by a VCC supply.

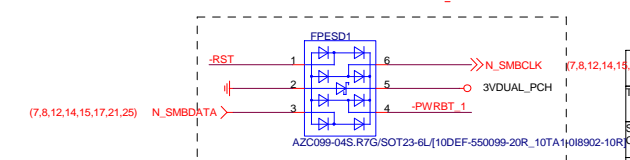
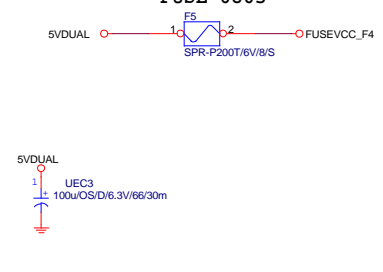
The schematic diagram illustrates the wiring for the Intel Front Panel connector. The F_PANEL header is connected to various system components and signals. Key connections include:

- VCC** and **5VDUAL** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- MPD-** and **PD+** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- 3VDUAL_PCH** connection to pin 14.
- HD+** and **HDLED** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- HD-** and **MSG/PD+** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- MSG/D-** connection to pin 4.
- PW+** and **PW-** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- PWRT** connection to pin 14.
- SP+** and **NC** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- SPK-** connection to pin 14.
- PD+** and **MPD-** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- PW+** and **PW-** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- PWRT** connection to pin 14.
- SP+** and **NC** connections to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20.
- SPK-** connection to pin 14.

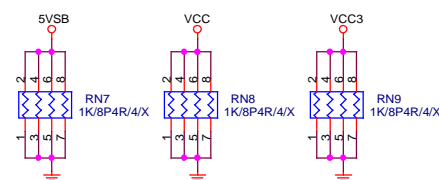
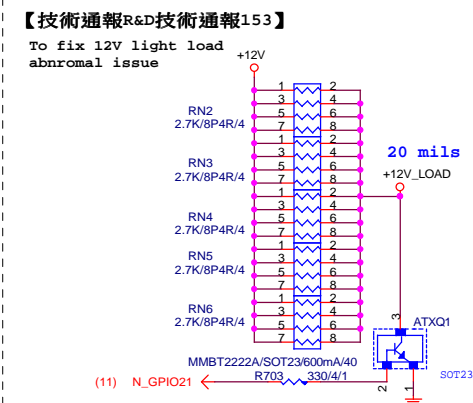
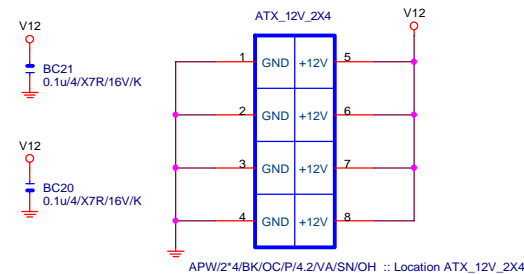
The diagram also shows the connection of the front panel to the system bus via the BH2*10K12.13/BK2.54/VA/PA connector.

Close to connector

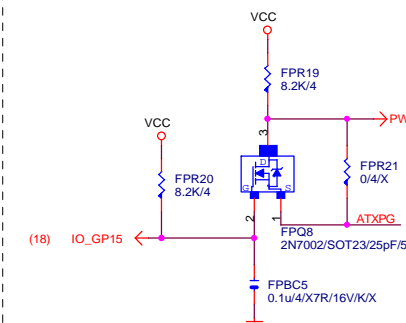
FUSE-0805



ATXX4 POWER CONNECTOR

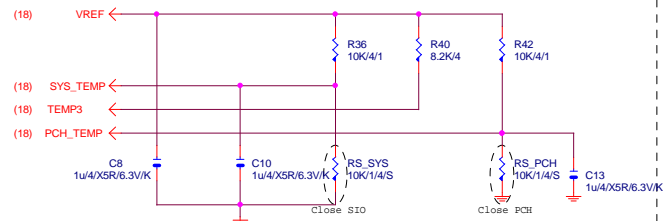


【技術通報R&D技術通報154】

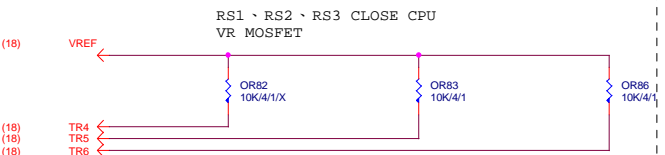
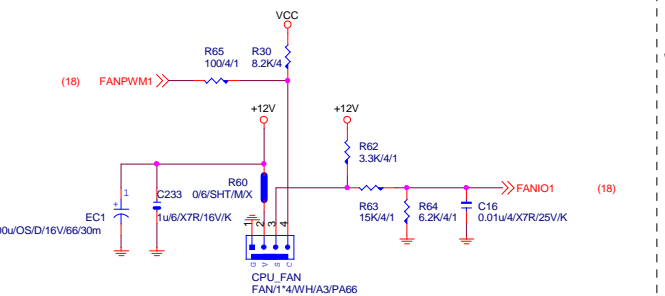
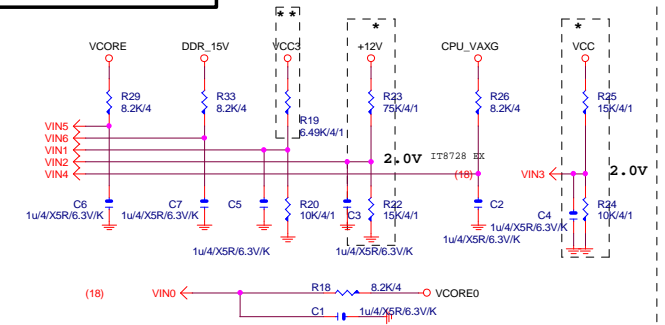


Title			
ATX,CLOCK GEN ,M3 POWER			
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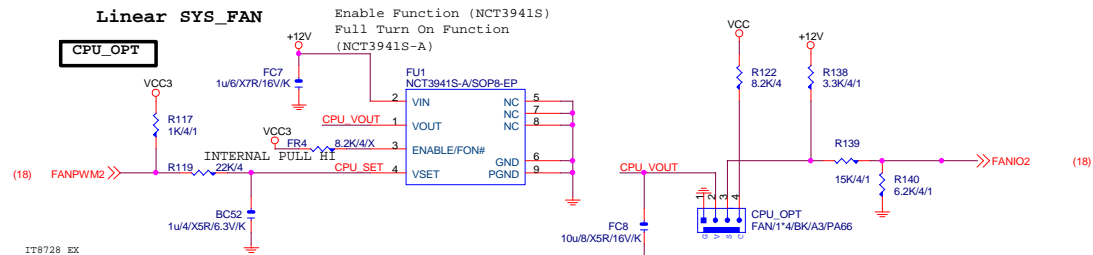
TEMP H/W MONITOR



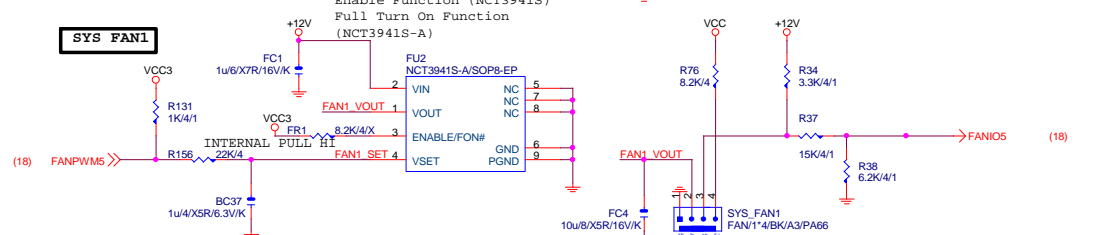
VOLTAGE-- H/W MONITOR



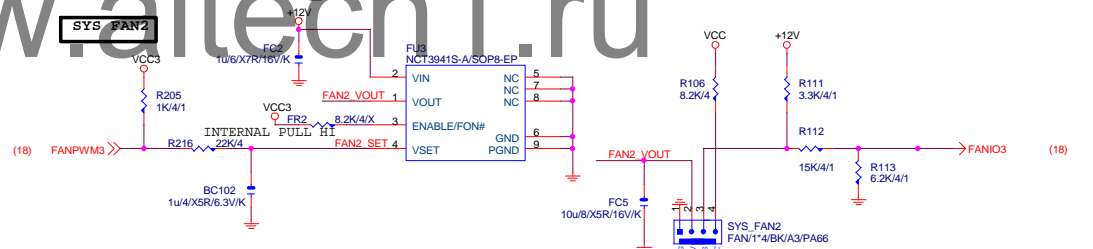
Linear SYS_FAN



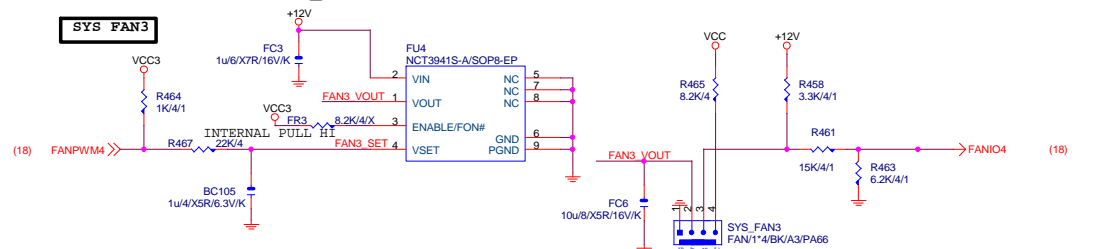
Linear SYS_FAN



Linear SYS_FAN



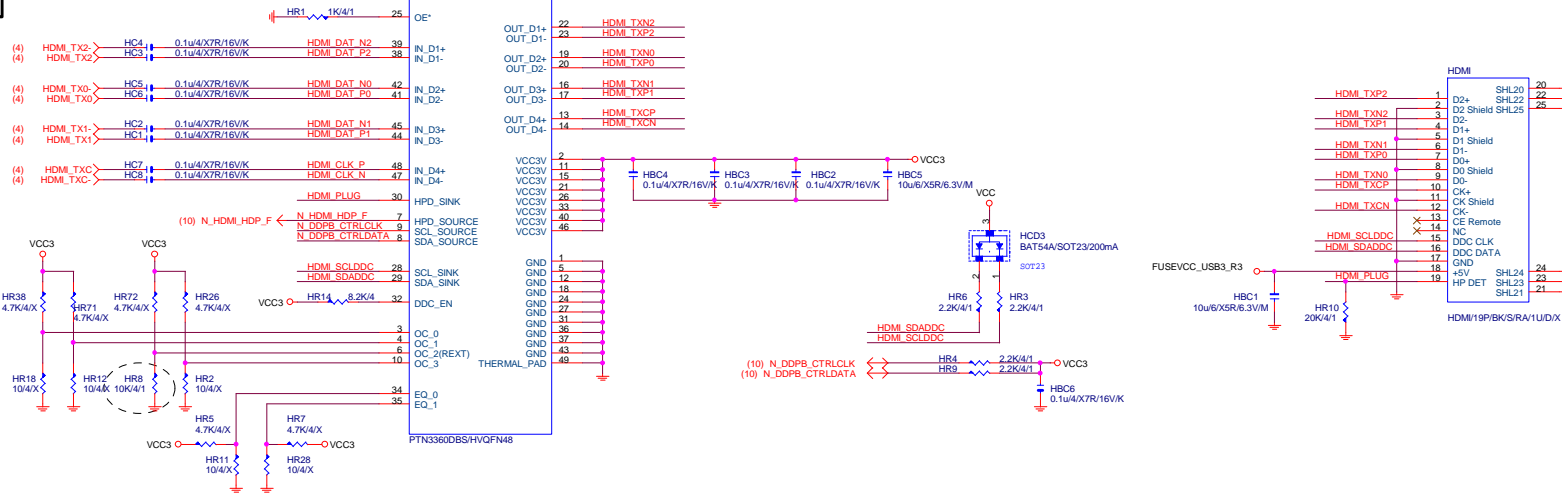
Linear SYS_FAN



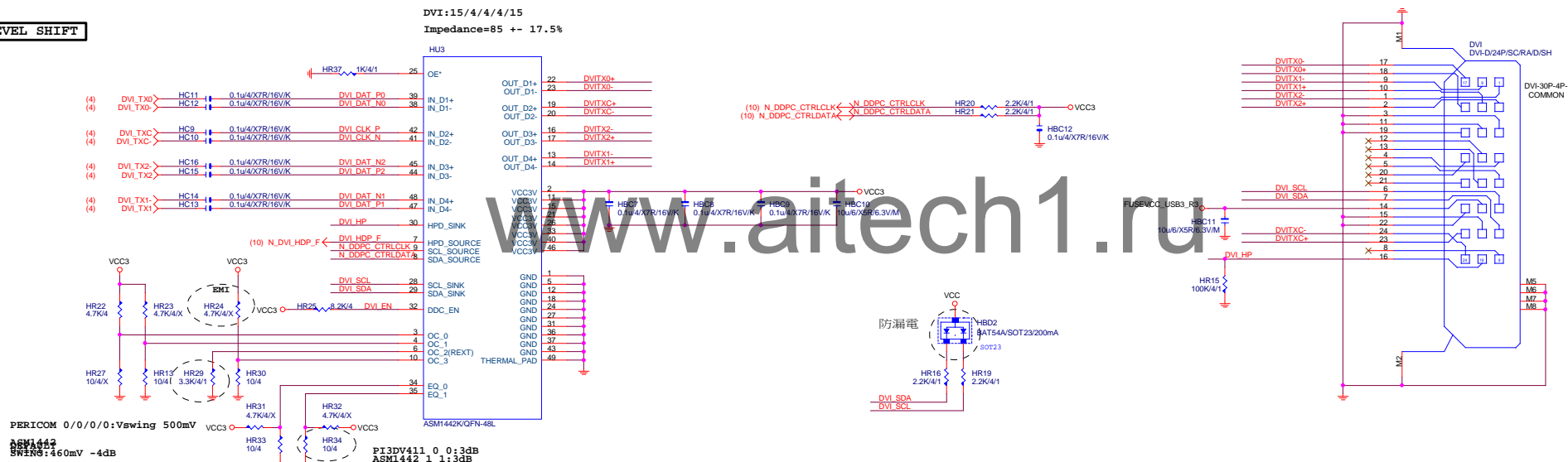
Gigabyte Technology

Title			HWM, FAN CTRL
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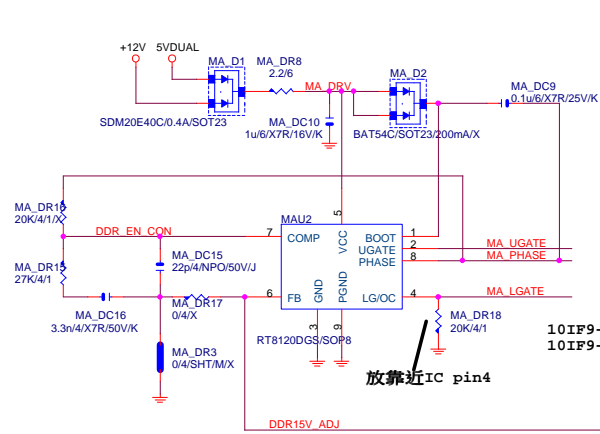
HDMI LEVEL SHIFT



DVI LEVEL SHIFT



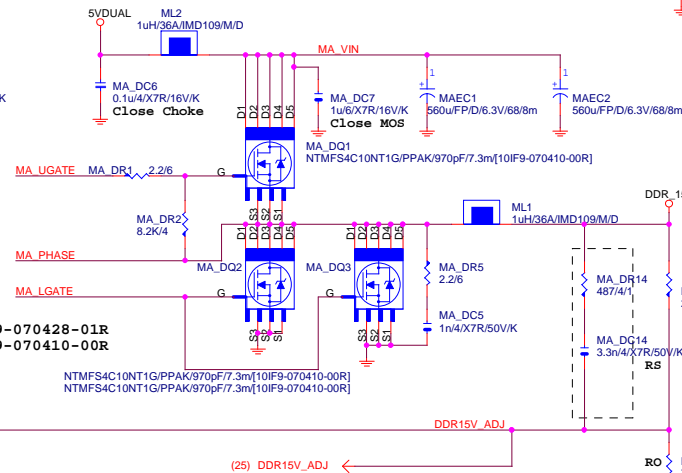
DDR_15V



(18) DDR_EN_CON >> DDR_EN_CON

10IF9-070428-01R
10IF9-070410-00R

放靠近IC pin4

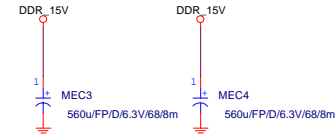


VIN=5V, VOUT=1.5V, IOUT=25A, PHASE=1
IRMS=11.45A

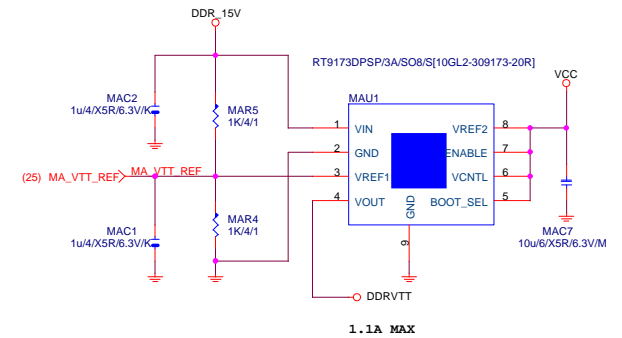
560u/FP/D/6.3V/68/8m RIPLE CURRENT=4.7A
Coefficient=1.7(85°C), 1(105°C)

VIN Ripple current=4.7X1.7=7.99A(85°C)
-->故固態電容須2X7.99=15.98>11.45A

OCP:35.82A for Rds=6.7m for vishay@4.5V
OCP:72.727A for Rds=3.3m for renesas@10V
OCP:48A=RoSet*Iocset / Rds(on)
=12K*10uA / [5//5]



DDR_VTT



Remote sense請從最重的負載端點拉回

$$0.8 \cdot (1 + RS/RO) = V_{out}$$

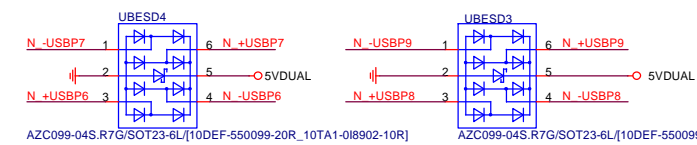
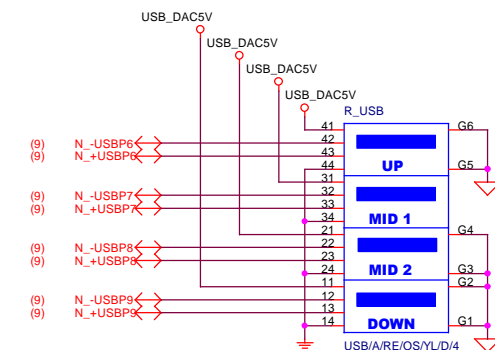
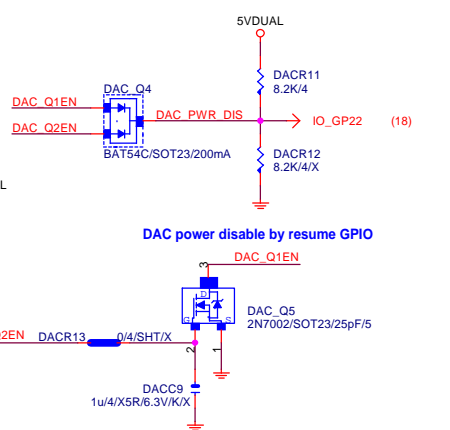
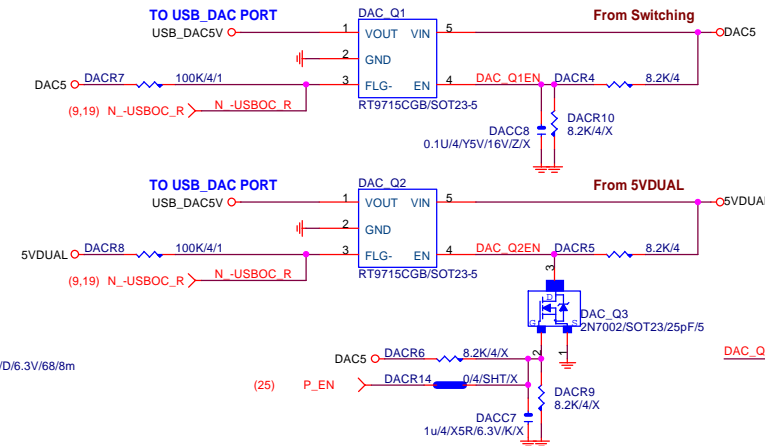
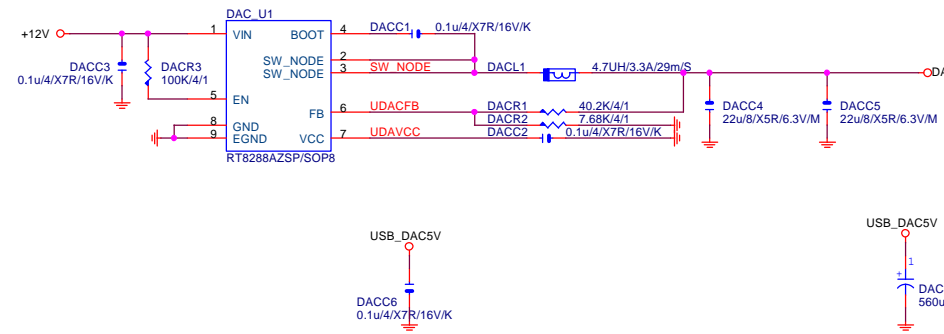
$$0.8 \cdot [1 + 2K/2.2K] = 1.527V$$

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USB_DAC



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